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Mini Review

A Roadmap for Disruptive Applications and Heterogeneous Integration Using Two-Dimensional Materials: State-of-the-Art and Technological Challenges

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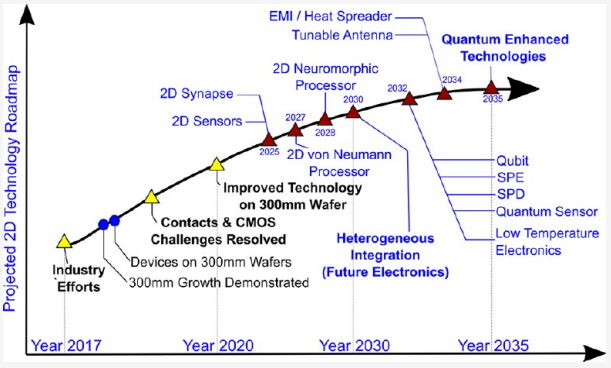
ABSTRACT: This Mini Review attempts to establish a roadmap for two-dimensional (2D) material-based microelectronic technologies for future/disruptive applications with a vision for the semiconductor industry to enable a universal technology platform for heterogeneous integration. The heterogeneous integration would involve integrating orthogonal capabilities, such as different forms of computing (classical, neuromorphic, and quantum), all forms of sensing, digital and analog memories, energy harvesting, and so forth, all in a single chip using a universal technology platform. We have reviewed the state-of-the-art 2D materials such as graphene, transition metal dichalcogenides, phosphorene and hexagonal boron nitride, and so forth, and how they offer unique possibilities for a range of futuristic/disruptive applications. Besides, we have discussed the technological and fundamental challenges in enabling such a universal technology platform, where the world stands today, and what gaps are required to be filled.



KEYWORDS: *Two-Dimentional Materials, 2D, Graphene, TMDCs, h-BN, MoS_2, Phosphorene, Heterogeneous Integration, Disruptive Technology, Universal Technology Platform*

1. BACKGROUND

The evolution of semiconductor technology, particularly the Si technology, has been a critical driver for the technological advancements that we see around us. The Si industry has come a long way from using 2250 transistors in Intel's 4004 (1971) to 11.8 billion transistors in Apple's A14 Bionic microprocessor (2020). A lot has changed over the years, not just in terms of the number of transistors per unit area and frequency of operation but also in terms of desired functionalities and applications given the nature of products that demand heterogeneous capabilities. In the future, therefore, the silicon-based technologies or, in general, the conventional bulk semiconductor technologies will find it challenging to meet the future technology requirements. The projected future requirements demand technologies such as flexible and wearable electronics, bioimplantable and flexible neuromorphic processors, terhertz (THz) electronics, multi-dimensional sensors and sensory systems, and quantum-enhanced systems for computation, sensing, and communication. Among various emerging materials, two-dimensional (2D) materials promise to offer solutions to existing issues/bottlenecks with conventional bulk platforms. They open opportunities for a plethora of new/disruptive applications and henceforth possibilities of new markets. This review aims to evaluate the potential of 2D materials for future technology applications. Also, it highlights the technical challenges required to be addressed in the future and sets a roadmap for 2D material-based electronics, optoelectronics, and quantum technologies, leading to heterogeneous integration.

2. TWO- DIMENSIONAL MATERIALS AND THEIR UNIQUE PROPERTIES

Although there are more than 130 materials that are found to be thermodynamically stable in 2D form, graphene transition metal dichalcogenides (TMDCs), hexagonal boron nitride (h-BN), and phosphorene are the leading materials due to their extraordinary electronic and optical properties.[1−8] Some of these properties include the following: (i) their bandgaps are tunable and lie in different regions of the electromagnetic (EM) spectrum, as depicted in Figures 1 and 2, which makes them suitable for a range of optical applications; (ii) these materials offer carrier mobility equivalent to or better than their bulk/thin-film counterparts, as depicted in Figure 2a, which makes them

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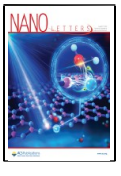

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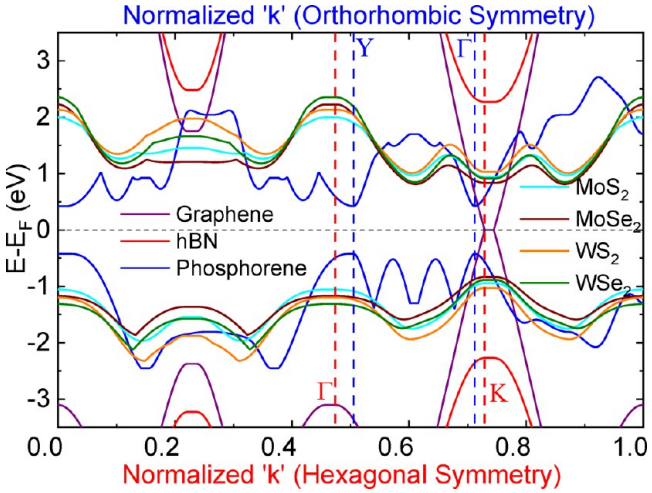

Figure 1. Band structure comparison of graphene, h-BN, phosphorene, and TMDCs. k-axis has been normalized to adjust all of the plots in the same frame. Only VBM and CBM of all of the elements are shown in the figure.

suitable for miniaturized high-performance electronics; (iii) some of these materials offer very high thermal conductivities (e.g., graphene and h-BN); and (iv) the majority of the 2D materials offer high sensitivity toward several volatile organic compounds (VOCs) making them suitable for sensing applications. Other than classical applications, these materials have also emerged as potential materials for enabling quantum technologies and quantum-enhanced applications. The fundamental properties of some of the materials are reviewed below by using density functional theory-based computations. The computational method used here is explained in detail in our earlier works.[9]

2.1. Graphene. Graphene[1,2] is a monatomic sheet of carbon (C) atoms having a highly symmetric hexagonal lattice (Figure 3a). Each carbon atom in graphene's lattice is bonded with three nearest carbon atoms through an in-plane σ bond, resulting in an sp^2 hybridization with a C—C bond length ~1.42 Å. C—C also results in an out-plane π-bond, contributing to a delocalized electron cloud across the sheet, like metal. Because of symmetry, π and π^* orbitals meet at "K" point known as Dirac cone and result in a zero bandgap in graphene (Figure 3b). Graphene also has linear dispersion near the Dirac point. Thus, it has zero effective mass, which is why graphene offers significantly higher electrical conductivity (mobility) and thermal conductivity. Strong in-plane symmetric C—C bonds also provide a high in-plane tensile strength to graphene sheets. Two atoms per unit cell result in six vibrational modes for graphene (Figure 3c). Out of the six modes, three are acoustic (LA, TA, and ZA) modes. The other three are optical (LO, TO, and ZO) modes. LA and TA show liner dispersion relation, whereas ZA shows quadratic dispersion relation near Γ-point. LA and TA have a relatively higher slope (i.e., photon velocity), which results in graphene's high in-plane thermal conductivity. Graphene does not have an energy gap between acoustic and optical modes, making graphene a fast heat spreading material. For bilayer (BL) graphene, its band structure is a little dispersive near the Dirac cone (Figure 3b). However, it still shows zero bandgap. Yet, its effective mass increases due to nonlinear dispersion near the K-point. The slope of the acoustic phonon dispersion curves (i.e., phonon velocity) is higher in BL graphene (Figure 3d) when compared to ML graphene. This makes BL graphene offer a better thermal conductivity as compared to monolayer graphene despite increasing its effective electronic mass. It should be noted that the bandgap of graphene can be tuned by introducing unique defect sites in the lattice, as disclosed by Kumar et al.[9]

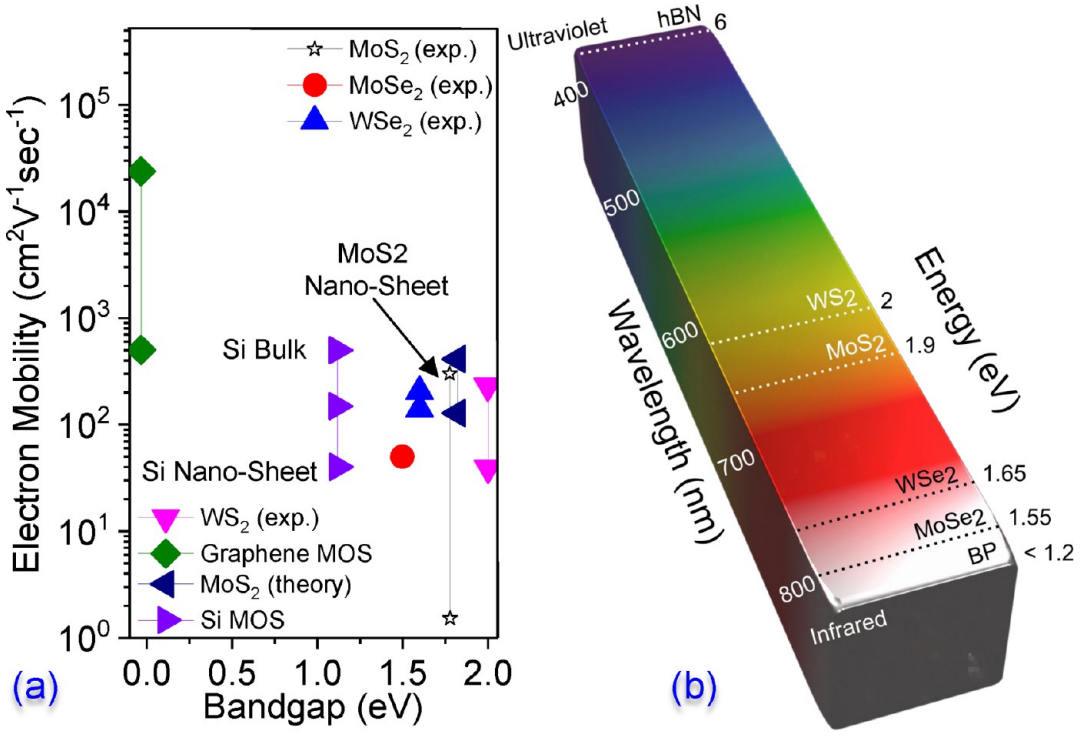

Figure 2. (a) Electron mobility versus electronic bandgap of various 2D materials and its comparison with Si in its bulk as well as thin film form. (b) Chart depicting the wide range of optical spectrum (from far-infrared to deep ultraviolet) which 2D materials cover.

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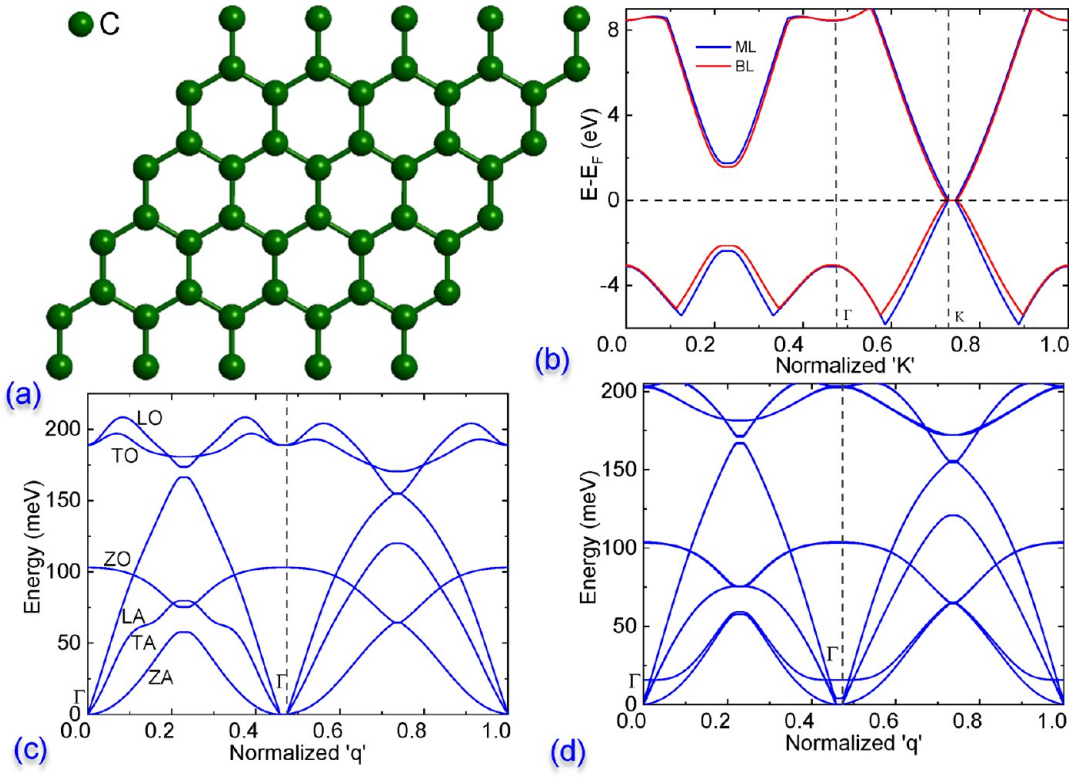

Figure 3. (a) Hexagonal lattice of graphene. (b) Electronic band structure of ML and BL graphene. Phonon band structure of (c) ML graphene and (d) BL graphene.

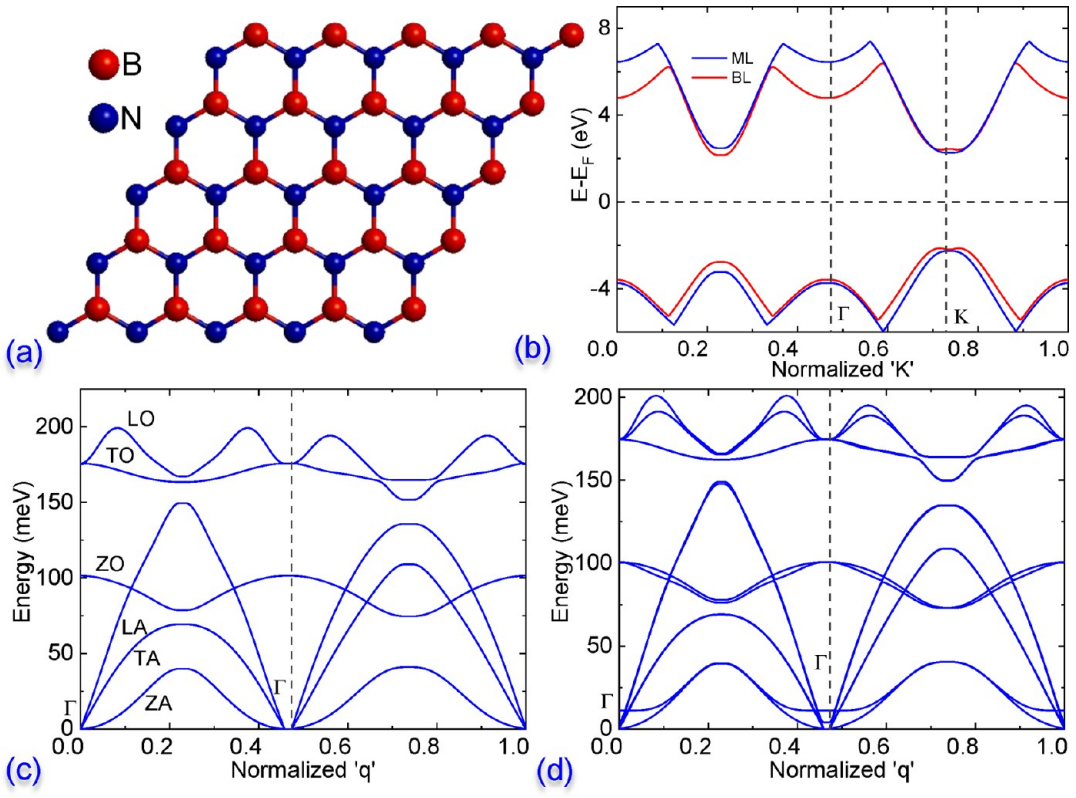

Figure 4. (a) Hexagonal lattice of h-BN. (b) Electronic band structure of ML and BL h-BN. Phonon band structure of (c) ML h-BN and (d) BL h-BN.

2.2. Hexagonal Boron Nitride. Hexagonal boron nitride (h-BN)[3,4] is a monatomic sheet, like graphene (Figure 4a) where each boron atom is bonded with three nitrogen atoms and vice versa in the monatomic plane. Here B—N bond length is ~1.45 Å. h-BN offers a direct bandgap at the K-point (Figure 4b) with a bandgap >5 eV, making it an electrical insulator.

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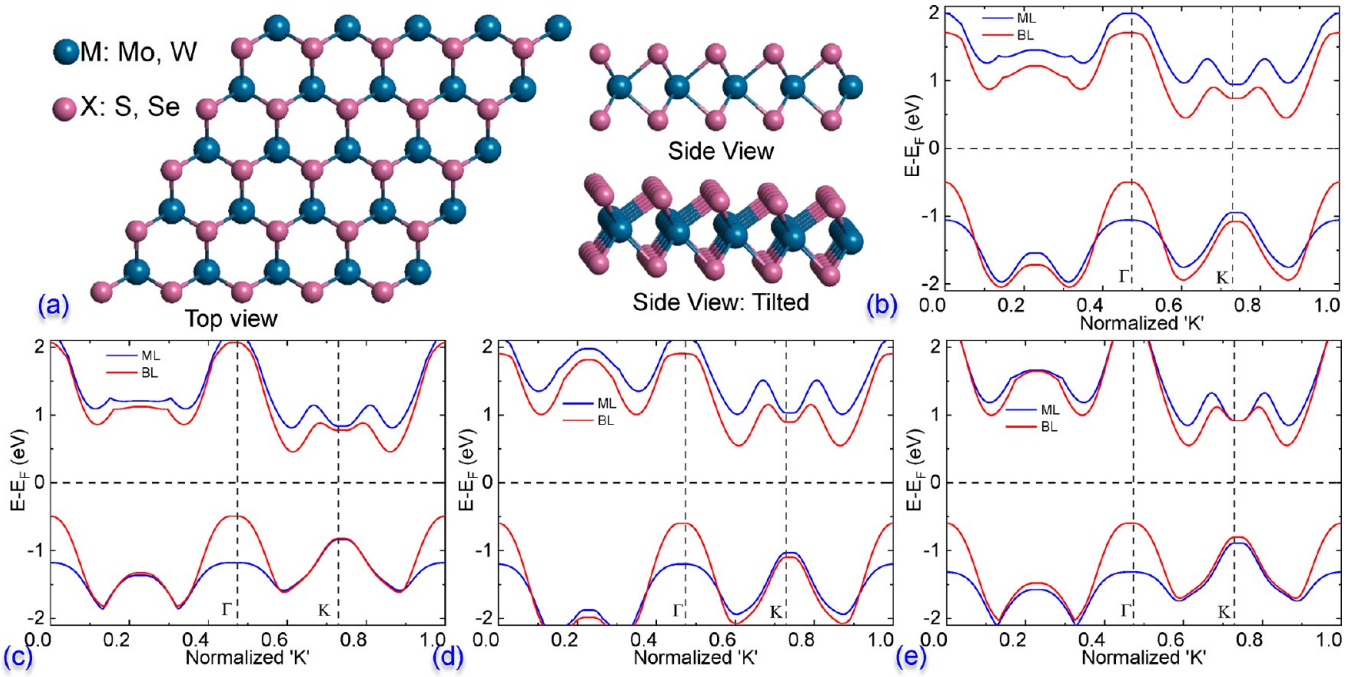

Figure 5. (a) MX_2 crystal structure. Top view depicts hexagonal lattice symmetry. Electronic band structure of monolayer (ML) and bilayer (BL) (b) MoS_2, (c) $MoSe_2$, (d) WS_2, and (e) WSe_2.

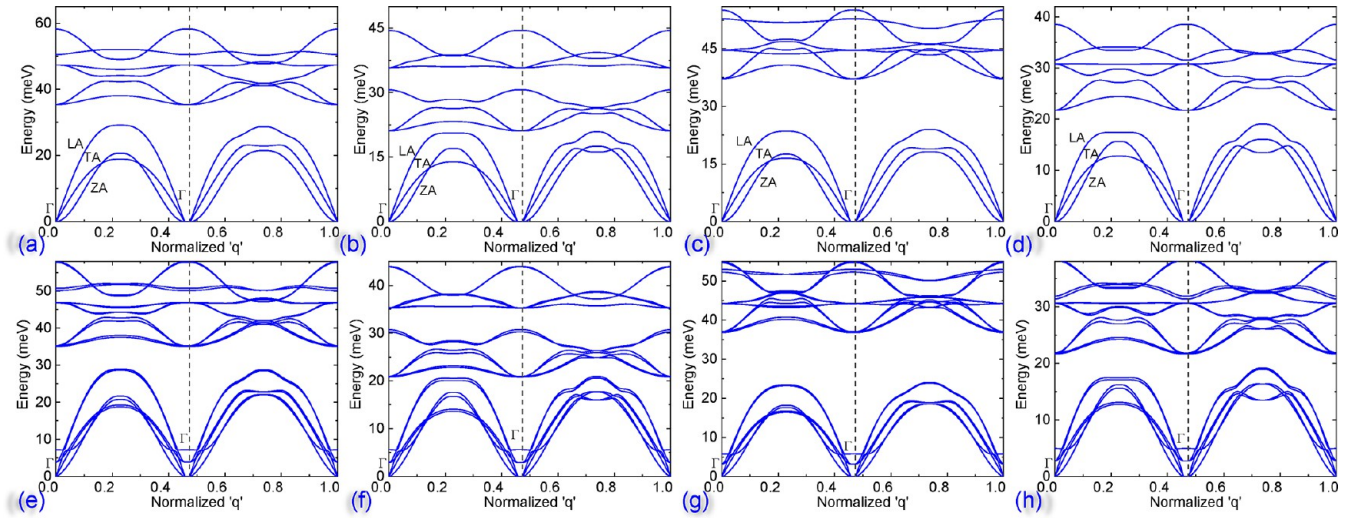

Figure 6. Phonon band structure of monolayer (a) MoS_2, (b) $MoSe_2$, (c) WS_2 and (d) WSe_2. Phonon band structure of bilayer (e) MoS_2, (f) $MoSe_2$, (g) WS_2, and (h) WSe_2

Strong in-plane bonds provide high tensile strength to h-BN, like graphene. Although h-BN is an electrical insulator, it has high thermal conductivity due to LA and TA phonon modes (Figure 4c). Bilayer (BL) h-BN does not significantly differ in its band structure near the K-point (Figure 4b). Thus, the electrical and optical properties of a bilayer and monolayer h-BN do not significantly differ. However, the thermal conductivity of BL h-BN increases due to its higher acoustic phonon velocity (Figure 4d).

2.3. Transition Metal Dichalcogenides (TMDCs). Transition metal dichalcogenides (TMDCs)[5−7] is a triatomic layer sheet with hexagonal lattice symmetry. It has MX_2 stoichiometry, where a metal (M) layer is sandwiched between two chalcogens (X) layers (Figure 5a). Although a range of materials falls under this category, MoS_2, WS_2, $MoSe_2$, and WSe_2 have been explored significantly compared to other similar materials. In the trilayer sheet, one chalcogen atom is bonded with three metal atoms, and one metal atom is bonded with six chalcogen atoms. Monolayer TMDCs offer a direct bandgap of around 1.5−2 eV near the K-point (Figure 5b−e). The band structures show significant curvature near the K-points, unlike graphene, which implies that the TMDCs have a higher electron/hole effective mass than graphene. TMDCs do not have in-plane bonds, which means the M−X bonds can be easily distorted by in-plane tensile stress. Hence, TMDCs have relatively weak mechanical strength compared to their monatomic layer counterparts like h-BN and graphene. TMDCs have nine vibrational modes due to three atoms per unit cell. Out of the nine modes, three (LA, TA, and ZA) are acoustic modes, and the other six are optical modes (Figure 6a−

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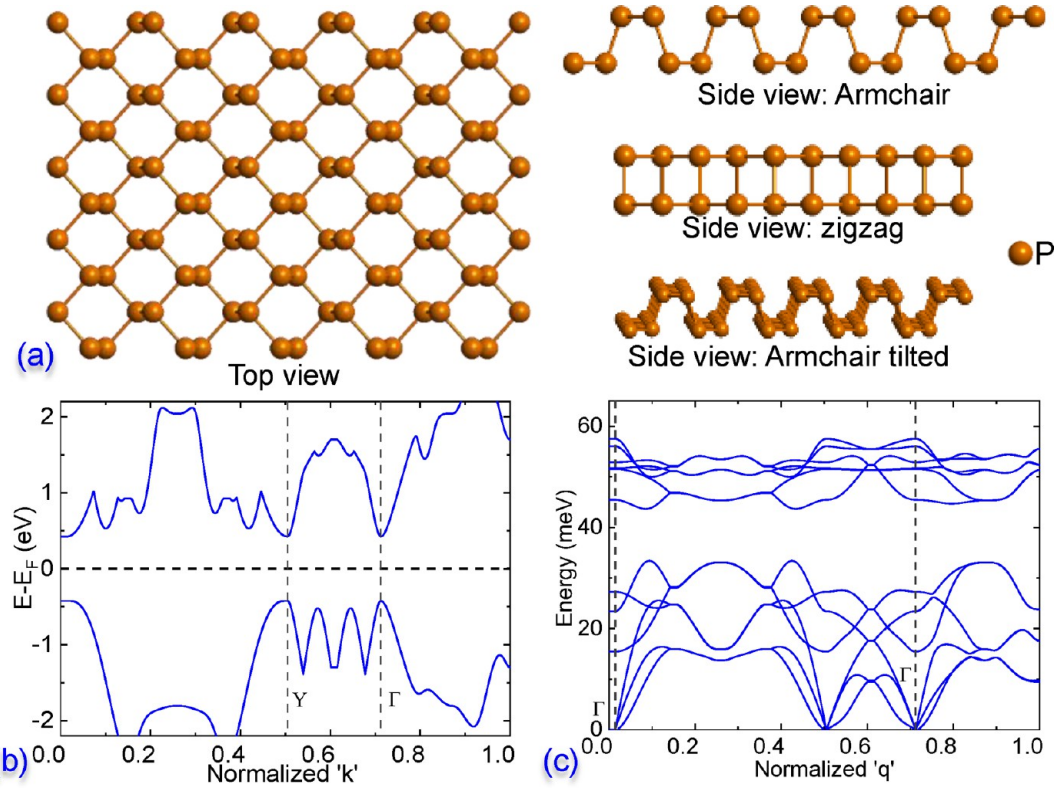

Figure 7. (a) Crystal structure of phosphorene. (b) Electronic band structure of ML phosphorene. (c) Phonon band structure of ML phosphorene.

d). The phonon velocity of the acoustic phonons is relatively lower in TMDCs, which implies that the TMDC thermal conductivity is lower than graphene and h-BN. A higher number of optical phonon modes also increase the probability of electron−phonon coupling in TMDCs, which lowers the carrier scattering time (τ), mean free path, and saturation velocities. TMDCs have a significant energy gap between acoustic and optical phonon modes, unlike graphene and h-BN, which lowers the rate of optical phonons to decay into acoustic modes, that is, lowers the heat dissipation capability. Because of lesser carrier scattering time and higher effective mass, TMDCs offer lesser carrier mobility than graphene. However, the mobility is high enough when compared to thin-film mobilities of conventional bulk materials. Besides, its direct tunable bandgap makes this material suitable for a range of optoelectronic applications. In the case of the bilayer (and few layer) TMDCs, valence band maxima (VBM) were found to be at the Γ-point with a lower gap than VBM at the K-point, while the conduction band minima (CBM) also moved away from the K-point with a reduced gap (Figure 5b−e). Thus, the material becomes indirect with a reduced bandgap, which degrades its optical properties though, and increased curvature near CBM improves its electronic properties. The optical phonon modes/population also increases (Figure 6e,f) due to the increase in the number of atoms per unit cell, which can adversely affect the transport properties due to increased scattering rate.

2.4. Phosphorene. Phosphorene[8] is a puckered bilayer sheet of phosphorus atoms which form an orthorhombic lattice structure. Phosphorus atoms in phosphorene are sp^3 hybridized, bonded with two in-plane (zigzag line) phosphorus atoms and one phosphorus atom in another plane (armchair line) (Figure 7a). P—P bond lengths are ∼2.22 Å and ∼2.24 Å in zigzag and armchair directions, respectively. P—P—P bond angles are ∼96.33° and ∼102.09° in zigzag and armchair directions, respectively. Phosphorene experiences intrinsic strain due to lesser P—P—P bond angle than typical sp^3 hybridized structures (∼109.5°). Attributed to these aspects, phosphorene has an anisotropic structure; hence it has asymmetric thermal and electrical properties in zigzag and armchair direction. The intrinsic strain and availability of a loan pair at each phosphorus atom make phosphorene unstable in ambient environments. Phosphorene band structure calculations show a direct bandgap of ∼1 eV near the Γ-point (Figure 7b), whereas its experimentally reported bandgap is ∼1.5 to ∼2.0 eV. Phosphorene has 12 vibrational modes due to 4 atoms per unit cell. Out of the 12 modes, 3 are acoustic modes, and the other 9 are optical modes (Figure 7c). Phosphorene retains its direct bandgap nature when number of layers are increased which offers an advantage over TMDCs, particularly for optical applications. However, its instability in the ambient condition is a big hurdle toward enabling such applications.

Further, the electrical, thermal, and optical properties of these 2D materials and performance figures of merit are quantitatively compared in Tables S1 and S2. The outnumbered electrical, optical, and thermal properties and performance figures of merit open possibilities for unique and disruptive applications as discussed in the subsequent sections.

3. UNIQUE AND WIDE RANGE OF APPLICATIONS OF 2D MATERIALS

3.1. Disruptive Applications Enabled by Graphene's Unique Properties. Fascinating electrical and thermal properties of graphene, as summarized in Tables S1 and S2, make it a potential material for ultrahigh frequency RF electronics, having operating frequencies above 500 GHz. Theoretically, graphene-based FETs can work as an active device for frequencies up to 20

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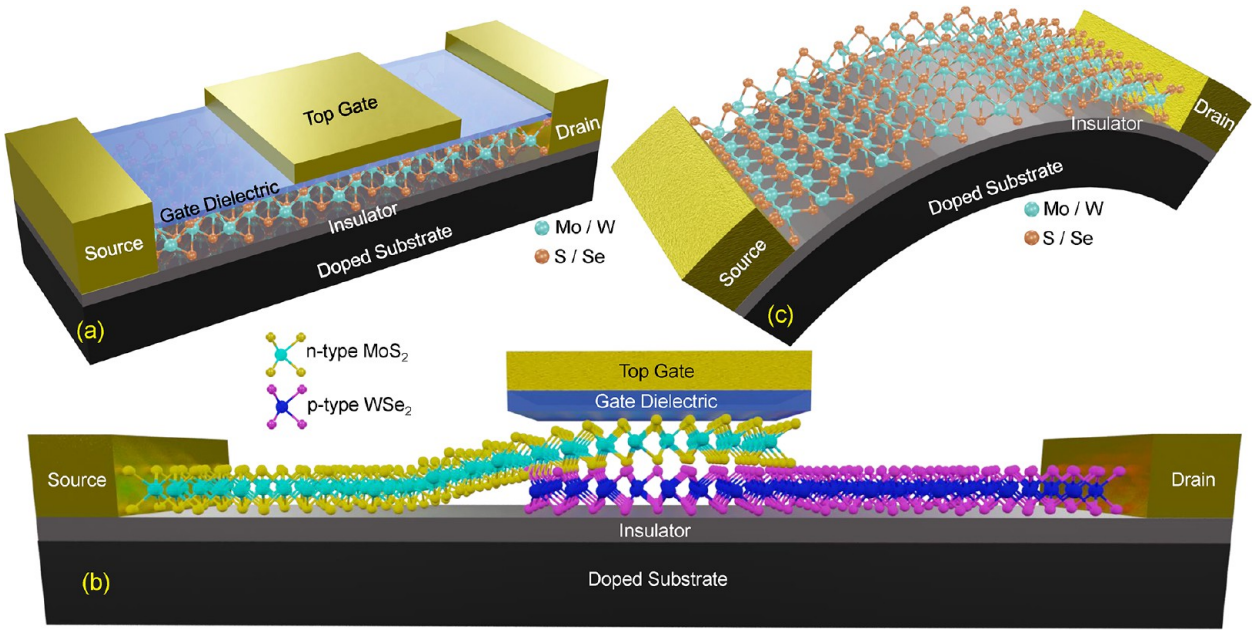

Figure 8. Isometric (atomistic) view of (a) 2D TMDC based top gates MOSFET, (b) TMDC heterostructure based tunnel FET, and (c) 2D TMDC based flexible FET. For clarity, top gate is not shown in (c). However, it is worth highlighting that flexible FET would also have the same gate stack configuration as it is in (a).

THz.[10] At present, there has been no other material discovered which has the potential to replace graphene's promise, thanks to its high carrier mobility, very high thermal conductivity, and saturation velocity (or higher mean free path). Such ultra-frequency electronics is projected to be useful in high altitude communication, on-chip wire-free interconnects, space missions, remote sensing, THz imaging, and so forth. Compared to conventional metals or graphite, graphene's extremely high thermal conductivity makes it a suitable material for heat spreading applications. Current handheld/mobile products use bulky graphite sheets as an on-board heat spreader. Graphene-based ultralightweight and high thermal conductivity heat spreader is of particular interest in future handheld/mobile products, projected to have a higher component density on board and are required to be sleeker as well as lightweight. Moreover, due to its ability to absorb and reflect electromagnetic radiation graphene is also a promising material for electromagnetic interference (EMI) shielding in electronic products, particularly future handheld/mobile products. Furthermore, graphene is also a promising material for interconnect applications, thanks to its excellent electrical and thermal conductivities. The semimetal nature of graphene and tunability of its conductivity as a function of the applied electric field normal to its conducting plane (e.g., via a back gate) make it an attractive material for tunable antenna applications, particularly for on-chip applications and for very high-frequency transmission. Graphene is transparent to visible light which makes it a suitable candidate for transparent displays. Furthermore, its transparent nature and significantly high mechanical strength open possibilities for large area foldable/bendable transparent displays on plastic. Attributed to its large surface to volume ratio, graphene's applicability in ultrahigh density supercapacitors, as well as molecular sensing applications, has already been established.

3.2. Sub-5 nm System-on-Chip (SoC). OFF-state leakage, short-channel effects like drain induced barrier lowering (DIBL) or threshold voltage roll-off, lower I_{ON}/I_{OFF}, and subthreshold slope (SS) $\gg$60 mV/decade are well-known trade-offs of channel length scaling. There are two potential ways to address these for high-performance sub-5 nm CMOS operation. One is to use an ultrathin body channel and high-k gate dielectric in conventional thermionic injection-based n-type & p-type FETs. Conventional bulk semiconductors experience a significant loss in carrier mobility, as depicted in Figure 2a, which is attributed to boundary scattering in bulk semiconductors. Boundary scattering however does not dominate carrier mobility in the case of 2D semiconductors. Furthermore, low electron (hole) effective mass in bulk semiconductors when compared to 2D materials in conjunction with quantum confinement lowers the density of states or maximum possible carrier concentration, when channel thickness is scaled below 3 nm. Moreover, quantum confinement increases the threshold voltage significantly, which lowers the gate swing and makes the transistor ineffective. Finally, lower body thickness also leads to non-idealities across the surface, which affects the channel properties and mitigates the gate oxide reliability. On the other hand, 2D materials, particularly TMDCs, due to their layered nature allow atomically thin and defects/dangling bond-free surface. Besides, 2D TMDCs due to their high effective mass do not suffer from quantum confinement or carrier loss like issues which are present in bulk semiconductors when thinned down to 2−3 nm. These attributes enable ultrathin body channel with body thickness as low as 0.7 nm with high channel mobility and integration of high-k gate stack without serious reliability concerns. An example 2D TMDC based short-channel FET is depicted in Figure 8a having a metal source/drain and high-k metal-gate stack.

The other approach uses tunnel FET architecture (TFET), which works on the principle of minority carrier tunneling from source to channel under a vertical (gate) electric field. This architecture is fundamentally free from the 60 mV/decade limit due to its tunneling nature and can be scaled significantly without serious short channel effects. Because of their defect-free atomically smooth surface and ability to form hetero-

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structures of 2D materials (spaced by a van der Waals gap), the 2D materials are among the most promising materials for TFET applications. The most basic TFET architecture, as depicted in Figure 8b, for n-FET operation requires a p-type 2D layer, stacked below an n-type 2D layer, where the n-type layer is connected to the drain terminal and the p-type layer is connected to the source terminal. A gate is further integrated over the n-type layer. Increasing gate voltage will accumulate additional electrons below the gate in the n-type layer. It will also enhance electron injection from the p-type layer into the n-type layer, thereby increasing the source-to-drain electrons' conduction. The p-channel FET is complementary to n-channel FETs. In recent years, 2D material-based tunnel FETs have seen decent progress; however, the performance is not on par with ultrascaled 2D TMDC based MOSFETs. For example, Sarkar et al. have shown a vertical TFET, realized using the heterojunction of a highly doped germanium (Ge) region and atomically thin MoS_2.[11] In another work, using a vertical heterostructure of $SnSe_2/WSe_2$ gate field-induced control over the band alignment was shown, which allowed tuning of the energy band offset from staggered type to broken gap type. Minimum SS of 37 mV/dec with high ON/OFF-current ratio ($\sim 10^6$) and high ON current was reported.[12] Several other works have also demonstrated TFET operation using heterostructures of $WSe_2/SnSe_2$, BP-$SnSe_2$, MoS_2-WSe_2, $MoTe_2-MoS_2$, and BP-MoS_2.[13−17]

3.3. Flexible Electronics. The desire to reduce weight and make electronics flexible without losing performance increases in areas of portable electronics, wearable electronics, IoT, RFIDs, flexible displays, and bioimplantable chips, to name a few commercial venues. For flexible electronics, the choice of materials must retain its electronic, thermal, and optical properties under various situations such as high bends or folds leading to strain exceeding 10%. Traditional electronic materials are brittle and prone to mechanical failures. Organic materials, while having mechanical flexibility, show poor electronic, optical, and thermal properties. On the other hand, due to high mechanical flexibility or bendability without losing their properties, 2D materials are therefore potential materials for developing flexible transistors (Figure 8c), which can enable future flexible electronics applications. Because of these attributes, several demonstrations have shown the promise of 2D materials for flexible electronics, sensing, and wearable applications. For example, graphene-based sensors mounted over a patient's tooth for detecting oral bacteria[18] were demonstrated recently. Graphene/h-BN heterostructures for wearable applications were printed on textiles, which did not lose their properties even after several washes.[19] Graphene tattoo sensors for monitoring temperature, hydration, ECG, EMG, and EEG over skin have also been successfully demonstrated.[20] Similarly, feasibility level studies using graphene and 2D TMDCs for flexible electronics are also in place;[21,22] however, the material quality and process technology on flexible substrates need to significantly improve if 2D material-based flexible electronics has to replace conventional electronics. This is attributed to high performance and high yield requirements for electronics applications. The material platform for applications like flexible sensors, bioimplantable, and wearable applications is usually low-cost printed or transferred polycrystalline films of 2D materials[23] and therefore is reasonably matured.

3.4. Nanoscale Memories and Synapse Using Resistance Switching in 2D Transition Metal Dichalcogenides (TMDCs). There are two different approaches to enable memory operation using 2D material-based devices. One is the conventional floating gate memory device (Figure 9a) or a charge trapping device, as discussed in ref 24. The other approach is to use resistance switching behavior present in 2D TMDCs, as illustrated in Figure 9b. After the experimental demonstration of the first memristor device in 2008 using a thin film of TiO_2,[25] it turned out that resistive switching is a common behavior in metal-oxides and similar dielectrics, which is fundamentally attributed to the migration of vacancies under an externally applied electrical field. Soon after discovering 2D TMDCs, the resistance switching was found to be a common phenomenon in metal-chalcogenides. While the metal oxide-based memristors were vertical two-terminal devices, 2D TMDCs allow resistance switching to be exploited in lateral (in-plane) direction. The advantage of lateral memristors over vertical ones is the possibility of integrating a control gate into the memristor, which was not possible in metal oxide-based two-terminal vertical memristors. Reports on resistance switching in TMDCs came up in 2015 when Sangwan et al. demonstrated a grain boundary-induced memristance in polycrystalline (CVD) molybdenum disulfide (MoS_2).[26] The authors observed that the orientation of grain boundaries within the device channel results in unique resistance switching behavior. The key to resistance switching in these devices was the migration of sulfur vacancies along the grain boundaries. Grain boundaries (GBs) in MoS_2 can be randomly oriented, and a combined effect could be seen in the resistance switching phenomenon. This makes it highly unlikely to predict the behavior and obtain a repeatable memory state. Although the GB's effect and role on memristor action seem rational, memristors on GB-less single-crystal MoS_2 have also been explored. It was shown by Cheng et al. that MoS_2 single crystal in its 1T phase not only offers higher current but also exhibits resistive switching.[27] Authors attributed it to electrical field-induced crystal distortion and increased delocalization of electronic states leading to a low resistance state,

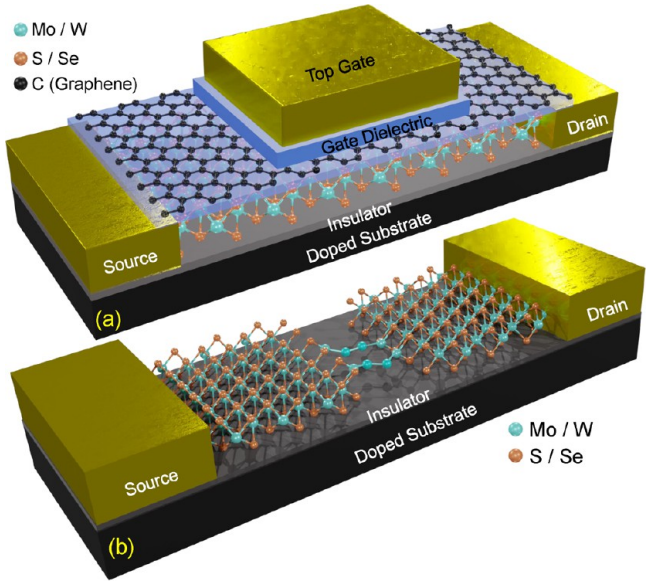

Figure 9. Isometric (atomistic) view of (a) 2D TMDC channel based floating gate memory where graphene is used as a floating gate between gate dielectric and blocking dielectric, and (b) TMDC channel based memristor in the programmed state. Memristor in its pristine/erase state is similar to a backgated FET, hence it is not depicted here

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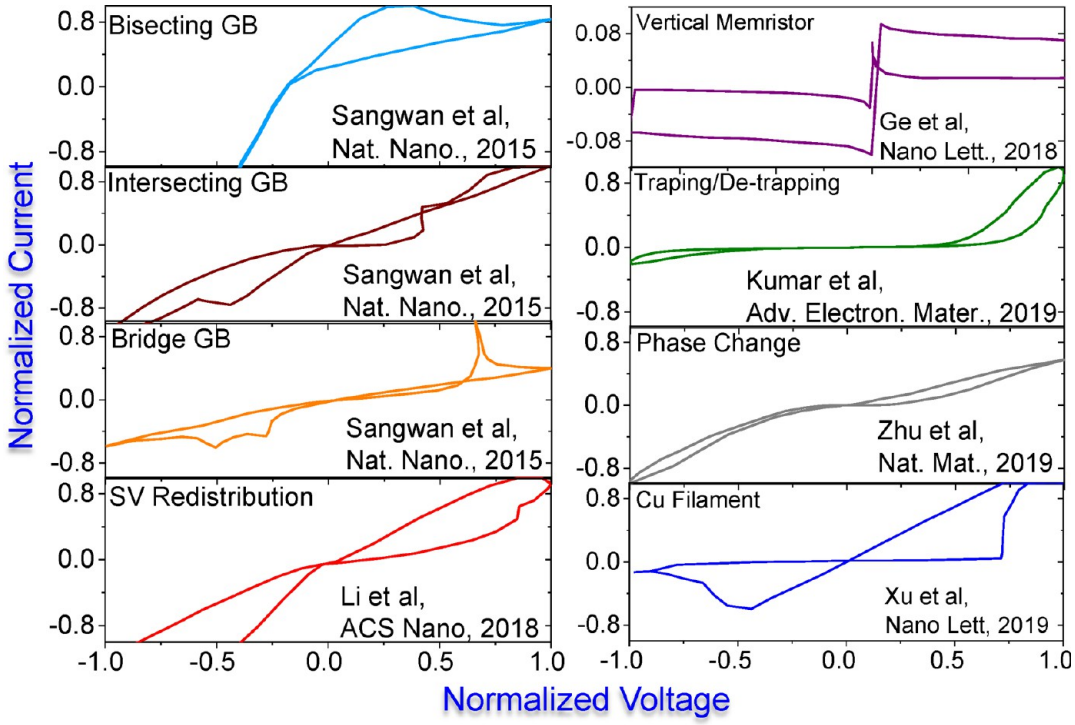

Figure 10. Current–voltage characteristics of TMDC-based memristors/resistive RAMs depicting unique RS mechanisms.

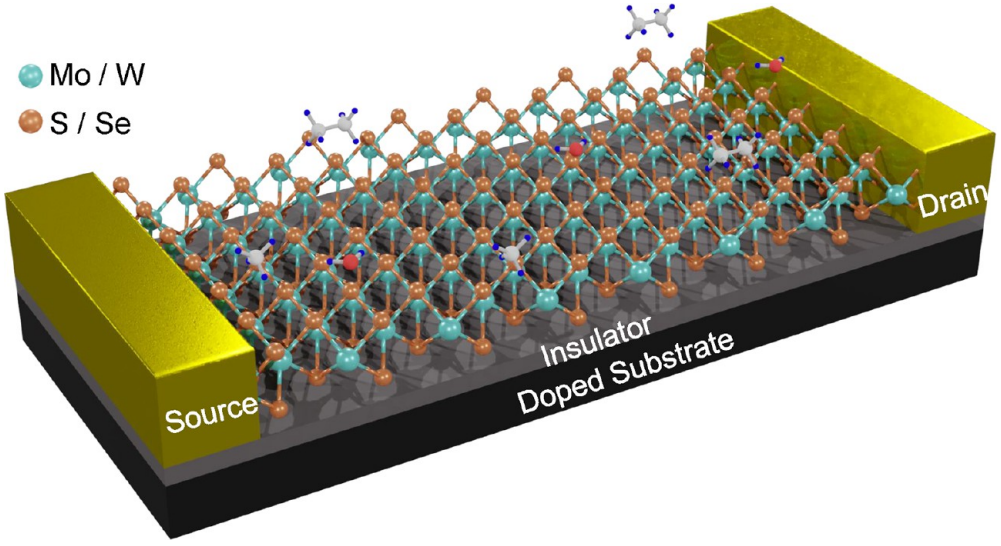

Figure 11. Isometric (atomistic) view of a 2D TMDC channel-based sensor. The illustration also depicts adsorbents adsorbed over the TMDC channel, which may change the electronic or optical properties of the channel and result in a change in electrical/optical signature post exposure to adsorbents.

which turns out to be reversible when the electric field direction was reversed. Meanwhile, vertical stacking of MoS_2 with other bulk materials was also shown to have resistive switching behavior.[28] Charge trapping/detrapping-induced resistance change is another mechanism by which the MoS_2 field-effect transistor exhibits memory behavior.[29] Chen et al. used plasma to create charge trapping sites on the surface of MoS_2 which led to a two-bit storage memory cell. With the application of a third terminal (i.e., gate), the cell was further modulated into multiple states. As far as crossbar integration of TMDC memristors is concerned, only vertical device structures have been used for such demonstration.[30] Vertical memristors are shown to exhibit low voltage resistance switching with a good enough dynamic range. Most of the memristors on TMDCs undergo resistance switching through anion migration or modulation of the Schottky barrier at the metal–TMDC interface. However, Xu et al. identified a different mechanism in MoS_2 memristors which exhibits resistance switching due to diffusion of Cu (contact electrode) in the vertical stack.[31] Another exception is the memristor action realized in MoS_2 FETs was by hysteresis engineering.[32] Typically, oxygen and moisture are responsible for charge trapping and detrapping during a gate voltage sweep, which results in significant hysteresis. Arnold et al. attempted to utilize this environment-induced phenomenon and mimic the

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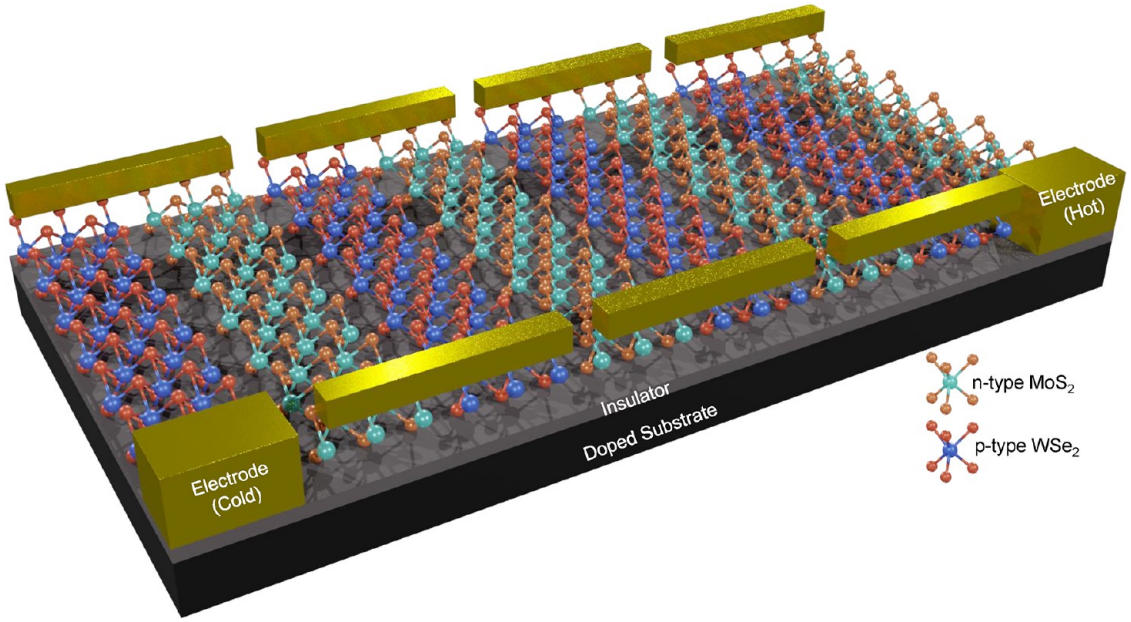

Figure 12. Isometric (atomistic) view of a 2D TMDC based thermoelectric device. Here p- and n-type channels are connected back-to-back (in series) between hot and cold electrodes.

neurotransmitter release as it happens in a biological synapse.[32] External stimulus like the light has been used by Yin et al. to enhance the switching ratio, thereby realizing a much wider memory window.[33] A few other reports on 2D TMDC based memristor are also available describing the resistance switching due to other factors.[34−38] While several reports showing unique current−voltage characteristics of TMDC RRAMs, as summarized above and depicted in Figure 10 below, suggest a possibility of multiple events being responsible for RS, a universal mechanism is yet not developed. It is important to note that different RS mechanisms result in varying magnitudes of the figure of merit parameters. While TMDC RRAMs, exhibiting filament formation, offer switching power as low as 0.01 fJ, those undergoing charge trapping/detrapping mechanism exhibit a large dynamic range (10^6) along with a relatively long retention time (∼10 000 s).[35] The principal advantage of using 2D RRAMs is to enable multibit storage and parallel computing through ultrascaled devices, especially when operated in a complex circuit of artificial neurons. However, incomplete insights on the physics of resistive switching (RS) in TMDCs continues to introduce device-to-device variation and hence failure in achieving the desired figures of merit like low switching power dissipation (<10 fJ), higher retention (>10 years), higher dynamic range (>10), and multibit programming states (>128).

3.5. Sensors and Sensor Arrays. Two-dimensional materials are among the most explored material for its application as a sensing device. Figure 11 depicts a typical 2D TMDC based sensing device. The interest in sensors is due to the 2D material's (i) high surface area to volume ratio; (ii) high carrier mobility when compared to organic counterparts; (iii) possibility to tune the channel's conductivity in the presence of an external (gate) field; and (iv) ability to functionalize the surface easily. Notably, 2D TMDCs offer a plethora of sensing possibilities due to their ability to introduce physical defects (vacancy or interstitial) and create unique midgap states through chemical functionalization of the surface, which offers distinct electrical responses to a range of volatile organic compounds (VOCs). Among various 2D materials, graphene[39,40] and MoS_2 have been the most explored materials demonstrating their ability to sense a range of VOCs. A few groups have also demonstrated the sensing ability of WS2, WSe2, PtSe2, SnS2, h-BN, and phosphorene. While 2D materials can sense a range of VOCs, achieving high sensitivity and selectivity are critical for 2D material-based sensors. The sensing ability is also seen to be intensely dependent on the quality of the material. While polycrystalline material or printed inks of 2D materials would result in sensitivity in the ppm range with response times in seconds, the same using high quality/defect-free CVD material results in ppb level sensitivity with a faster response time. So far, the majority of reports using 2D TMDCs are based on two-terminal resistive sensors (using $\Delta R/R$ as a metric); it is worth highlighting that 2D TMDCs also offer promise to realize FET-based sensors, which should improve the sensitivity by orders of magnitude. Selectivity, on the other hand, is a crucial issue required to be addressed. This can be addressed by (i) using single crystal CVD material while following a physics-based design approach to engineer the surface and midgap states and (ii) by deploying a sensor array where each sensor element uses a different functionalization scheme. Consistency, device-to-device variability, and response time are also key issues that can be addressed by (i) and (ii) listed above.

3.6. Thermoelectric. Several 2D materials have also been demonstrated to have viability for thermoelectric applications. Graphene, for example, has been a widely explored material before MoS_2. Seebeck coefficient (S) for graphene has been reported to be as high as 80 mV K^{-1} with thermal conductivity close to 5000 Wm K^{-1} at room temperatures. The same can be engineered further by the application of bilayer graphene.[41] In another work, power factor (10^{-2} W/mK^2) comparable to popular bulk Bi_2Te_3 with a maximum S value for monolayer (100 μV/K) as well as bilayer graphene (125 μV/K) was demonstrated.[42,43] Similarly, black phosphorus, attributed to its unique crystal structure, lower bandgap, and in-plane anisotropic properties, offers a Seebeck coefficient higher than graphene (335 μV K^{-1} for monolayer and 510 μV K^{-1} for few layers BP).[44] The same can be further improved by exploiting

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BP's anisotropic properties.[45] TMDCs, due to high electrical conductivity and low thermal conductivity, show high *S* values. Buscema et al. and Wu et al. reported tunable S for monolayer MoS_2 using external electric field[46] or gate field,[47] respectively. Figure 12 shows the isometric view of a 2D TMDC-based conventional equivalent thermoelectric device with p-type and n-type channels. Here p- and n-type channels are connected back-to-back (in series) between hot and cold electrodes resulting in an open circuit voltage in the presence of a temperature difference between hot and cold electrodes.

3.7. Optoelectronics. Typical optoelectronics devices are photodetectors and photoemitter (e.g., a light-emitting diode). A photodetector would result in a change in electrical response in the presence of light, often of a desired wavelength or frequency band. A photoemitter would emit a photon of the desired wavelength in the presence of a defined electrical impulse.

In the case of photodetectors, there are generally three types of architectures often explored. These are (i) a 2D TMD FET (Figure 13a), which works like a photodetector under OFF state; (ii) a three-terminal device (Figure 13b) consisting a 2D TMD layer placed over a backside gate, working as the source of an electron−hole pair (produced in the presence of photon impulse) and buried under an electron collecting 2D layer (e.g., graphene or phosphorene), wherein the electron collecting layer would be connected between a source and drain terminal; and (iii) a p−n junction formed by the heterostructure of different 2D materials (Figure 13c). In the case of (i), electron−hole pairs are generated under OFF-state operation of the 2D TMD FET when photons with energy higher than the bandgap are bombarded over the channel. Excess e−h pairs are seen in the form of increased OFF-state or leakage current. In the case of (ii), while the 2D TMD layer generates the e−h pairs, electrons are drifted toward the electron collecting layer, for example, graphene, and these excess electrons, that is, presence of photons, are seen in the form of an increased current through the graphene channel. In the case of (iii), the e−h pair is generated across a reverse-biased p−n diode, which is observed in the form of increased dark current or reverse leakage current in the p−n junction diode. The same if integrated over a backside gate gives additional advantages of improved sensitivity and bandgap tunability.

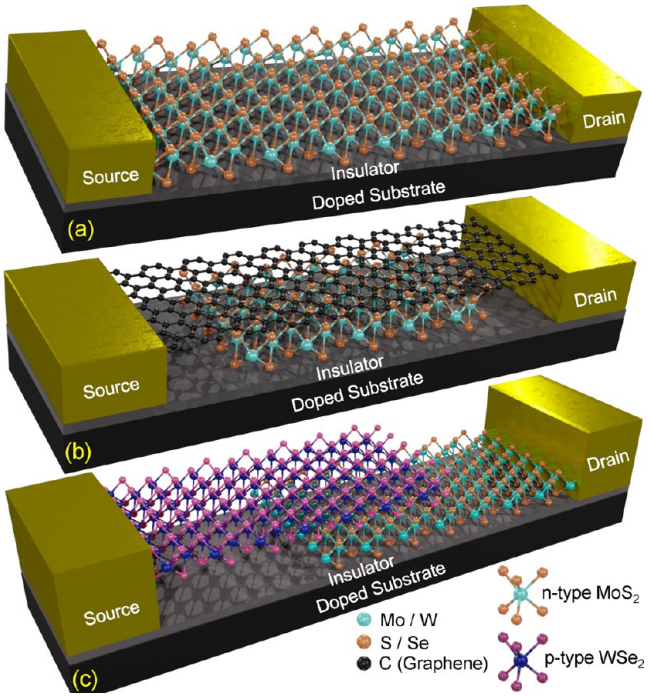

Figure 13. Isometric (atomistic) view of (a) 2D TMDC channel-based photodetector, (b) graphene−TMDC based photodetector, and (c) 2D TMDC heterostructure based photodetector.

As far as photoemitters are concerned, there are two key architectures often explored. These are (i) a p−n junction formed in a given 2D semiconductor, often a TMDC, through electrostatic doping (Figure 14a) and (ii) a p−n junction or quantum well formed by the vertical stacking of 2D materials having different properties (Figure 14b). In the case of (i), the two sides of the channel are electrostatically doped with electrons and by holes, by using respective back-gates biased at positive and negative voltages. When a lateral field is applied across the two sides to forward bias the diode, a recombination of electrons and holes at the p−n junction leads to photon emission. However, in the case of (ii), a heterostructure of 2D material forms a tunnel diode having minority carrier tuning from one layer to the other layer in the presence of an external bias, which leads to the formation of excitons causing photon emission.

3.8. Quantum Computing. The most fundamental building block of a quantum computer is a quantum bit (qubit). The 2D materials demonstrate rich physical phenomena and provide a favorable platform to explore interactions among various particles and quasiparticles. These interactions provide various ways to store data and therefore realize qubits. Two reasonably explored approaches for realizing these qubits using 2D materials are (i) quantum dot (QD) qubit (Figure 15a) and (ii) superconducting qubit (Figure 15b). While QD qubits are still at an exploratory stage, superconducting qubits, on the other hand, are commercially viable. The recent quantum supremacy demonstrations by industry were based on superconducting qubits.

The most popular material for realizing QD qubit, before 2D materials, was GaAs. GaAs qubits have short decoherence time due to spin−orbit interaction and interactions with nuclear spin. On the other hand, graphene QD qubits have weak spin−orbit coupling and have long coherence times.[48] The *g*-factor demonstrated by graphene QDs is ∼2, which is 5 times higher than GaAs QDs. However, while the weak spin−orbit coupling results in long spin decoherence times, it also makes the operations lower.[49,50] Apart from graphene, Coulomb blockade has been demonstrated in MoS_2, WS_2, and WSe_2 quantum dots.[51−53] TMDC QDs have large spin−orbit coupling that results in a large splitting of spin and valley degenerate states, which is theorized to offer long decoherence times for TMDC qubits. Encapsulated heterostructures of MoS_2, hBN, and graphene have been shown to provide additional performance improvement.[54,55]

A superconducting qubit consists of a dielectric sandwiched between superconducting components (metal) to form a Josephson junction (JJ), requiring a super clean interface between a dielectric and the superconducting metal. The 2D materials are atomically smooth and can offer such clean interfaces, which are devoid of dangling bonds, unlike its bulk counterpart (Al_2O_3). Besides, using a 2D material as the barrier material provides an added advantage of having gate-tunable transmon.[56] This gives an additional knob to engineer the ratio between Josephson energy and charging energy, which should

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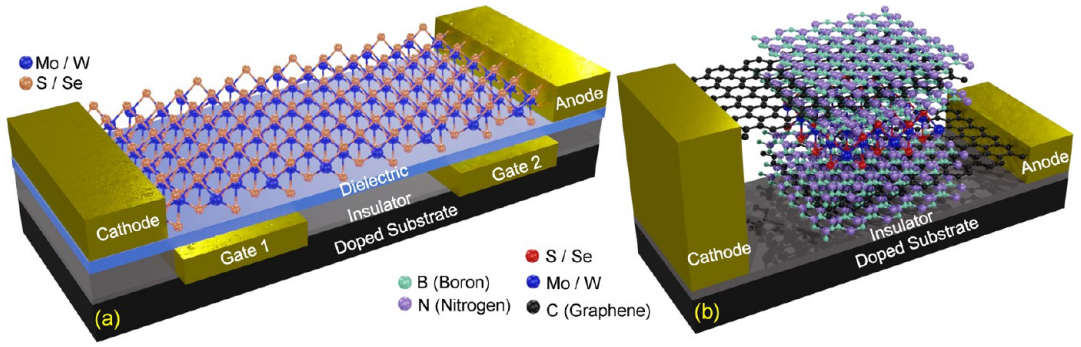

Figure 14. Isometric (atomistic) view of (a) electrostatically doped p−n junction-based photoemitter, (b) 2D heterostructure quantum well-based photoemitter.

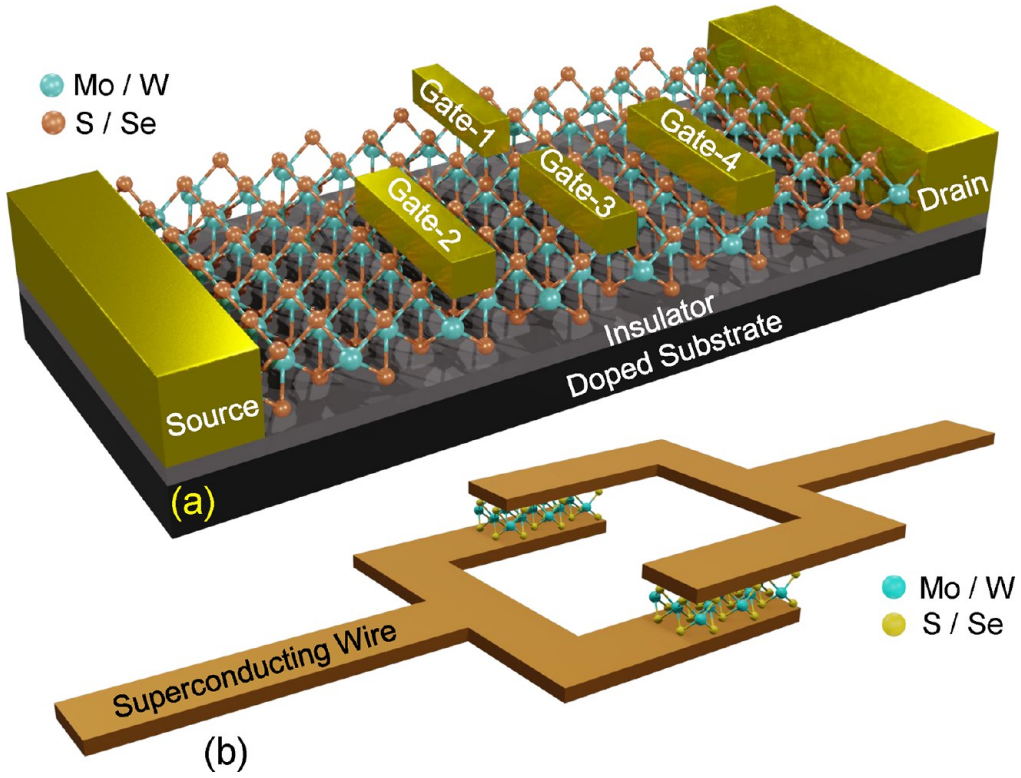

Figure 15. Isometric (atomistic) view of (a) quantum dot qubit where the carrier (electron) is trapped inside a electrostatically formed potential well within the 2D TMDC (or graphene) channel, and (b) superconducting/transmon qubit having 2D TMDC (or graphene) to form Josephson junction.

be high enough so that the anharmonic transmon is immune to perturbations.

Another emerging approach using 2D materials is to use its topological properties, which have been discovered in certain monolayer 2D TMDCs in their 1T′ phase.[57] In 2014, Qian et. al[57] demonstrated that single-layer TMDCs of the form 1T′-MX_2 are quantum spin Hall insulators where M = Mo and W, and X = S, Se, and Te, which can result in topologically protected edge-states that exhibit spin velocity locking. Since then several studies have been conducted by various groups to study topological properties of 2D materials, such as WTe_2,[58−61] $MoTe_2$,[62−64] and Bi_2Se_3.[65,66]

3.9. Quantum Communication. Advances in photonic technologies have led to quantum entanglement being utilized for instantaneous and fool-proof quantum secure communication over long distances. This technology's backbones are single-photon emitters (SPEs) and single-photon detectors (SPDs). Among possible materials, 2D materials, due to their properties being different from typical bulk materials, are of particular interest due to the unique quantum phenomena observed across these few atom thick layers. Among 2D materials, TMDCs and h-BN are of key interest, attributed to its thickness-dependent bandgap and optically coupled spin and valley degree of freedom. To date, single-photon emission has been demonstrated primarily on WSe_2, h-BN and $MoSe_2$. However, the progress on 2D material-based SPD is yet not significant except for improving the detection capability of 2D heterostructure-based photodetectors. In 2017, Walsh et al. proposed a graphene JJ-based SPD.[67] Theoretically, such a JJ SPD will be able to detect photons infrared to microwave regimes. Monolayer graphene has a relatively lower electron−phonon coupling and negligible electronic specific heat capacity than metals attributed to negligible density of states (DoS) near its charge neutrality point. Therefore, in case a single photon is absorbed by a graphene channel, it can heat the channel significantly. Sensing this short heat pulse in the form of change in current generated

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by a single photon is possible through such a graphene-based superconducting−graphene−superconducting Josephson junction SPD.

4. TWO-DIMENSIONAL TECHNOLOGY STATE-OF-THE-ART CHALLENGES AND WAY FORWARD

4.1. Two-Dimensional Material Growth. Chemical vapor deposition (CVD), molecular beam epitaxy (MBE), pulsed laser deposition (PLD), and atomic layer deposition (ALD) are the key methods demonstrated for the growth of 2D materials like TMDCs, h-BN, and their hetrostructures. For graphene however, CVD and MBE are the most popular techniques. CVD is a bottom-up approach for realizing thin films on the desired substrate. Typically, transition metal oxides such as MoO_3 and WO_3, halides like $MoCl_5$, and chalcogen powder (S or Se) are used as CVD precursors at temperatures exceeding 800 °C.[68] Growth reaction is limited either by mass transport or reaction rate depending on the temperature, vapor pressure, and pressure of the carrier gas, affecting the material quality. For example, gaseous phase precursors have shown much better uniformity of TMDC films than solid-state precursors.[69,70] Although high-temperature growth improves film quality, a low-pressure growth process facilitates controllable growth by enabling precise control over the concentration of precursor molecules. Choice of substrate is another important parameter that determines the quality and rate of the growth process. The most used substrates for TMDC growth are inert SiO_2,[71] mica,[72] polyimide,[73] and gold/tungsten foils.[74] Furthermore, to facilitate nucleation, organic molecules like perylene-3,4,9,10-tetracarboxylic dianhydride (PTCDA), reduced graphene oxide (rGO), and perylene-3,4,9,10-tetracarboxylic acid tetra potassium salt (PTAS) have been demonstrated as seeding promoters.[75] Besides, compounds like alkali metal halides, sodium cholate, and NaOH are used as growth promoters by forming volatile intermediates, thereby accelerating the formation of subsequent regions of the film.[76] Despite numerous growth methods for high-quality uniform TMDC films, deposition of large-area single grain/crystal TMDC has not been possible yet using conventional CVDs. Smaller grains are typically accompanied by a large density of grain boundaries, nonuniform layer thickness, contaminations, and chalcogen vacancies, which collectively degrade electrical and thermal transport properties. Several of these issues are addressed by another CVD technique, which uses metal−organic precursors like $Mo(CO)_6$ etc. (metal−organic CVD or MOCVD). The high vapor pressure of metal−organic precursors allows one to reliably set the concentration of gaseous precursor in the gaseous mixture by controlling the evaporation rates of the solid precursor.[77] It has been observed that much better control over GB concentration (grain size as large as 10 μm) can be achieved by exposing the substrate to nucleation suppressors such as alkali metal halides, together with the Mo precursor, before the growth stage.[77] As a result, MoS_2 films with a finite number of GBs (large grain sizes) are made plausible. Atomic layer deposition (ALD) is another growth method wherein a high-quality monolayer-by-monolayer deposition occurs via a self-limiting chemical reaction, thereby resulting in extremely precise control over the film thickness and uniformity.[78] However, reports on grain size controllability are missing. MOCVD is considered the best technique as we advance, which can enable growth over large size (200 mm and above) wafers.

MBE is a broadly accepted technique for the growth of uniform epitaxial thin films.[79,80] In MBE, a high energy electron beam is used to melt the elemental powder to produce the required precursor vapors. Precise control over the electron beam energy and the process at ultrahigh vacuum enable realization of uniform, high quality thin films. However, MBE growth of TMDs has been rather challenging, particularly on conventional substrates due to high melting point of transition metals and low sticking coefficient of S/Se atoms at ultrahigh vacuum. This results in smaller domain sizes and poor stoichiometry control at high temperatures, a condition necessary to promote surface diffusion. To alleviate this problem, use of van der Waal's substrates like mica, h-BN, epitaxial graphene, and HOPG is preferred over conventional surfaces/substrates like sapphire, GaN, SiO_2, and so forth. These van der Waal's substrates enhance surface diffusion of the transistor metals by reducing surface−precursor interaction. Use of layered substrates together with precise control over electron energy potentially makes MBE the ideal technique to realize high quality 2D material heterostructures.[2] However, large domain size and wafer-scale MBE are yet to be realized.

Pulsed laser deposition involves a high energy pulsed laser to form a plasma consisting ions and atoms which are eventually collected over a substrate placed near the target at a very high temperature. The quality of deposited film depends on various parameters like substrate temperature, laser power, laser wavelength, pulse duration, and so forth. Unlike other thin films, PLD growth of TMDCs is rather challenging due to the presence of two different element atoms. Typically, metal substrates like Ag is used to deposit high quality TMDC films due to the formation of Ag_2S, which acts as a template for TMDC growth.[81] However, the presence of native oxide on metal substrates prevents easy formation of TMDC films. Besides metal substrates, insulating substrates like Al_2O_3, GaN, SiC, sapphire, HfO_2, quartz, and SiO_2[82,83] also support deposition of 2D films at a relatively higher temperature. However, the processes of PLD-based 2D material growth is yet not understood completely; the reason why is that PLD growth of newer 2D materials is not trivial and requires rigorous optimization.

Apart from single layer TMDCs, the current state-of-the-art growth methods can realize vertical and lateral heterostructures. Vertical stacking of different 2D materials have been possible largely due to the lack of lattice matching requirements for these materials. The following four different kinds of vertical heterostructure combinations are possible so far: (i) semiconductor/semiconductor junctions having different semiconducting-TMDCs or semiconducting-TMDCs/phosphorene; (ii) metal/semiconductor junctions consisting of graphene semiconducting-TMDCs, metallic-TMDC/semiconducting-TMDCs, graphene/phosphorene; (iii) semiconductor/insulator junctions consisting of semiconducting-TMDCs/h-BN; and (iv) metal/insulator junctions consisting of graphene/h-BN. On the other hand, limited by strict lattice match requirements, lateral heterostructure growth of only few combinations is possible: (i) metal/insulator (e.g., graphene/h-BN), (ii) semiconducting/semiconducting (e.g., semiconducting-TMDC/semiconducting-TMDC) and (iii) semiconducting/metallic TMDC.[68]

4.2. Oxides/Dielectrics for 2D Material Channel. Layered 2D materials ideally provide a clean dangling bond-free interface that was expected to solve issues posed by downscaled bulk materials and surface dangling bonds.

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However, it was noticed that 2D materials are susceptible to adsorbed molecules or atoms over their surface. The sensitivity increases many folds if dangling bonds or vacancies are present over the surface. These adsorbed molecules could also be due to deposited oxide/dielectric or metal (for S/D contact). This can drastically affect the transport properties of the channel.[84] Therefore, the choice of dielectric material/insulators is crucial for efficient and reliable device design with a high degree of gate control. Besides, 2D material surface is not conducive to oxide growth, which further adds to the challenge in realizing a reliable gate stack or surface passivation scheme. The choice of gate dielectric is based on the following three factors: (i) easy growth/deposition over the surface, (ii) it must not lead to the creation of interface traps, (iii) it must passivate at trap states present at the surface due to surface defects, (iv) it must not functionalize with the surface atoms, and (v) it must not limit the channel mobility due to Coulomb scattering or optical phonon scattering. Figure 16 shows graphene FET's cutoff frequencies

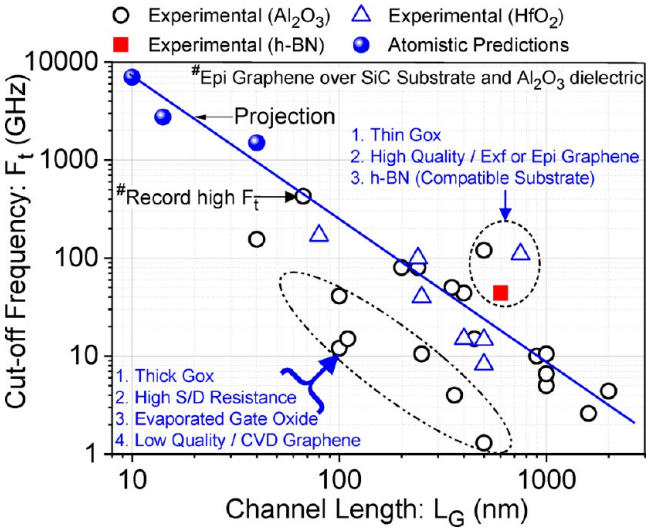

Figure 16. Cut-off frequency versus channel length of graphene FETs reported to date. Data is plotted for different gate oxides used.

reported to date as a function of channel length and different gate dielectrics used. The transistor's intrinsic performance is a strong function of the gate dielectric used. Choice of gate dielectric also affects the behavior of surface/interface traps, which shows up in the form of current−voltage (I−V) hysteresis and temperature instabilities. For example, h-BN can mitigate the I−V hysteresis, but the temperature dependence suffers due to the presence of thermally activated traps.[85] The defective gate dielectric can also lead to localized states, which are often theorized to be the origin of ambipolar conductivity in TMDC FETs.[86] Multilayer MoS_2 on PMMA and SiO_2 show ambipolar and unipolar behaviors, respectively, which was attributed to high mobility with long-range disorder domination in the case of PMMA and low mobility with short-range disorder dominating in the case of SiO_2 as the gate dielectric.[87] While h-BN and high-k dielectrics such as HfO_2, ZrO_2, and Al_2O_3 offer improved mobility due to suppression of Coulomb scattering and optical phonon modes, their integration is often difficult. For example, the growth of h-BN over other 2D materials is still a challenge; therefore, h-BN over 2D materials is not a wafer scalable option.[88,89] HfO_2 on TMDCs has a highly dissociative activation energy that leads to the formation of pits in the dielectric, which causes substantial gate leakage apart from nonuniform channel properties. Buffer layers of Mg, Al_2O_3, Y_2O_3 between HfO_2 and TMDCs would improve conformability leading to smoother interfaces. Recently, Y_2O_3/HfO_2 stack was shown to offer high-quality interfaces with low D_{it} (2×10^{12} cm^{-2} eV^{-1}), low SS (65 mV dec^{-1}), and high ON current (526 μA μm^{-1}).[90−92]

Other than oxide- or nitride-based insulative gate, solid electrolytic gate (and substrate) is another emerging approach. This approach is inspired from liquid gating technique in which an electrolyte polymer or liquid is used as a functional material to tune the inversion charge density in the channel. Electrolytic substrates/gate offer a better control over channel than the same offered by oxide-based substrates/gate, which help in lowering the required gate overdrive and improve subthreshold slope. Popular solid electrolytic substrates include LICGC (lithium-ion conductive glass ceramic), LaF_3 (lanthanum fluoride), $LiCl_4$(PEO), and so forth. For example, Alam et al. demonstrated n-type MoS_2 and p-type WSe_2 transistors on LICGC substrates with SS approaching 60 mV/dec and sub-1 V gate operation.[93] Zhao et al. presented graphene FETs realized over LICGC substrate with superior channel control/modulation resulting in a sheet charge concentration as high as 1×10^{14} cm^{-2}.[94] Wu et al. demonstrated MoS_2 FETs over LaF_3 substrate with high tunability of channel charge (up to 4.1×10^{13} cm^{-2}), high ON−OFF ratio (10^4−10^5), lower interface electron scattering, and a uniform potential distribution across the channel.[95]

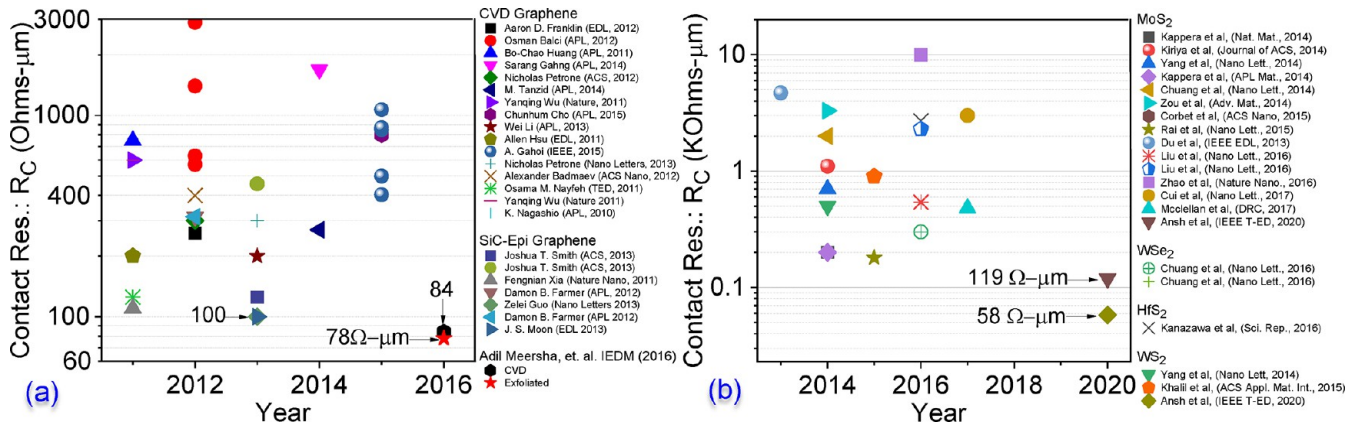

Figure 17. Contact resistance reported to date for (a) graphene−metal and (b) TMDC−metal contacts.

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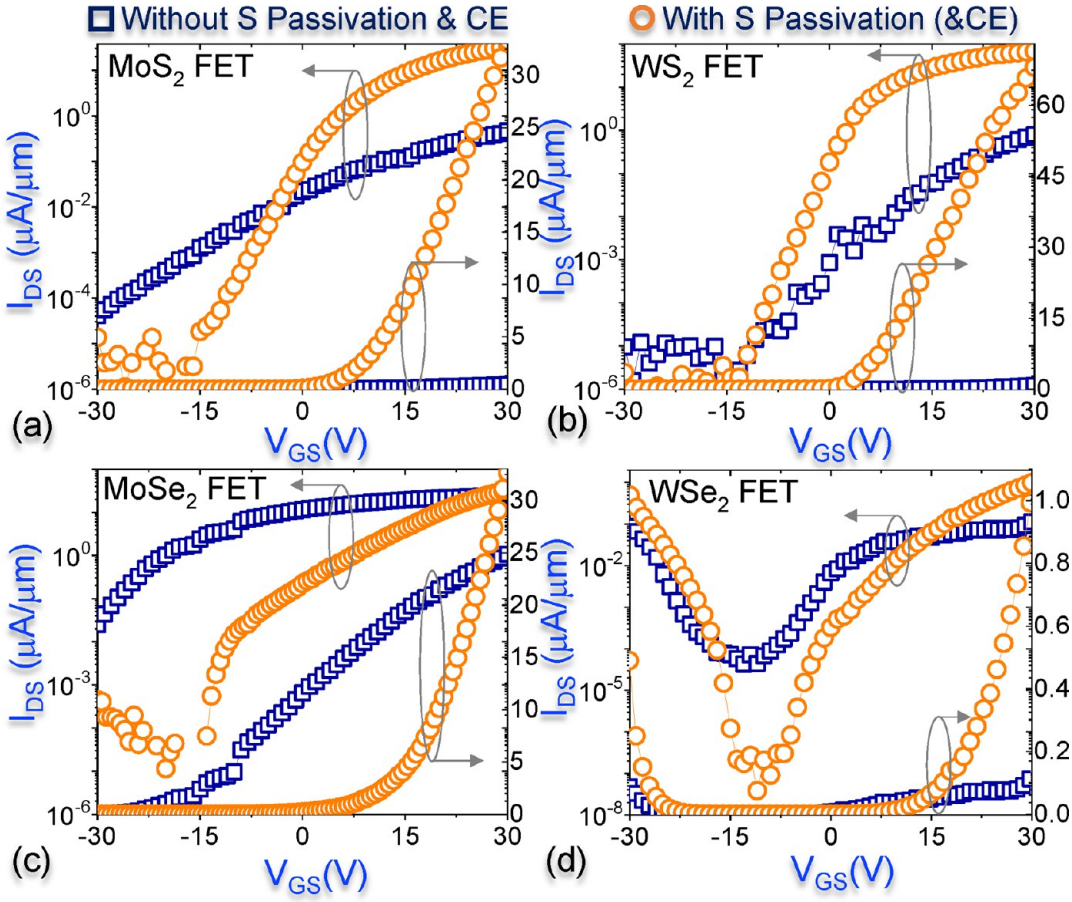

Figure 18. Impact of chalcogen-assisted channel passivation in four different TMDCs depicting improved ON-current, positive threshold voltage and suppressed OFF-state leakage in all the cases when the channel was passivated through a low-temperature H_2S treatment.[87]

4.3. Contacts and Its Quantum Chemistry. Metal−graphene and metal−TMDC contact resistance issues have remained a showstopper for several years, limiting one to exploit the intrinsic limits of these materials. Figure 17 shows the contact resistance reported to date for (a) graphene−metal and (b) TMDC−metal contacts. In the early years of development, graphene's and TMDC's contact resistance without contact engineering was typically found to be greater than 1 KOhms·μm. This is a value 20 times higher than typical contact resistance values in advance Si technologies. Only recently, by understanding the peculiar quantum chemistry of these contacts[96−99] does contact engineering in these materials became possible, which pushed the contact resistance values below the estimated fundamental limits derived from the Schottky−Mott formalism. The Schottky−Mott formalism defining the physics of charge injection across the metal−semiconductor interface becomes insufficient as the thickness of SC collapses to its 2D limit. This essentially means that when the thickness of SC is smaller or comparable to the typical width of the depletion layer or transfer length, the physics of charge injection at the metal−SC interface is determined by work function offset and the extent to which atomic orbitals overlap. This happens due to metal-induced changes in the electronic properties of 2D SC beneath the contact. Lack of dangling bonds perpendicular to the basal plane of the 2D channel prevents the formation of covalent bonds at the metal−2D SC interface and worsens the situation by limiting the interaction orbital interaction at the contact.[100] As a result, the 2D SC−metal contact, 2D TMDC−metal contact to be precise, suffers from Schottky barrier (SB) determined by Fermi-level offset and tunnel barrier (TB) introduced by noncovalent interaction between channel and contact metal. Moreover, Fermi-level pinning (FLP), commonly observed in bulk SC−metal interfaces, is found to strongly deviate SB height values from theoretical ones due to the presence of a large density of surface states.[101] Therefore, it is imperative to choose source/drain metal contact for 2D TMDC field-effect transistors (FETs) by looking at the work function alignment and the quantum chemistry between TMDC and metal. In principle, SB is reduced by reducing the density of surface states[102] and choosing metal with the lowest work function offset.[103] TB can be reduced by choosing metal contacts that exhibit maximum orbital interaction with the TMDC channel.[103] Athough SBH reduction has been demonstrated on multiple occasions by (i) degenerate doping of the contacts, (ii) weakening of FLP,[104] and (iii) choosing low work function metal for MoS_2, the reduction of TB is nontrivial as it depends not only on orbital level chemistry between TMDC and metal atoms but also on the character and density of surface defects. A general approach is to add interfacial defects of a certain kind to improve contact bonding. However, one needs to carefully understand the role of various kinds of defects, using quantum chemistry simulations, on charge distribution and sheet resistivity beneath the contact. A specific example is the introduction of S interstitial atoms via low-temperature annealing in an H_2S environment. S interstitial atoms were found to enhance charge sharing between the transition metal and contact metal, thereby significantly

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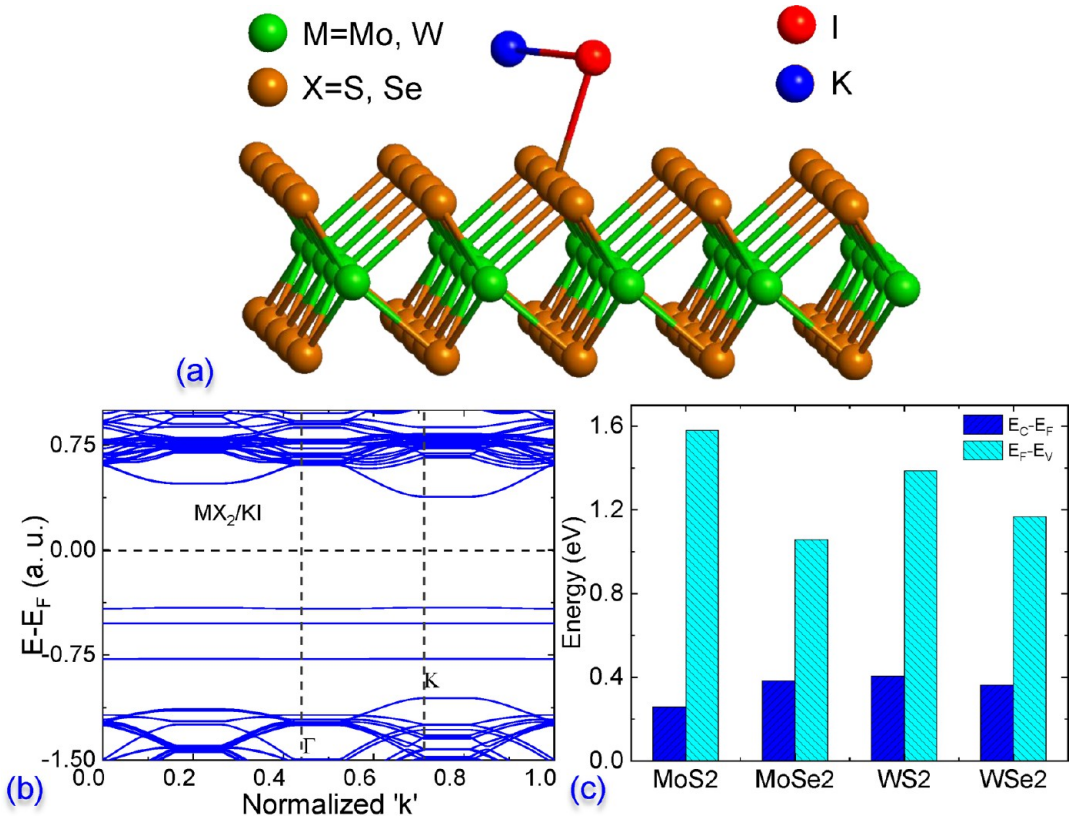

Figure 19. (a) KI adsorbed over the surface of TMDC channel. (b) Band structure plot depicting shift in Fermi energy resulting n-type doing. (c) Relative position of Fermi energy from conduction (and valence) band energy level after KI treatment in four different TMDCs.

improving the atomic orbital overlap at the contact and improving contact properties. Such a technique has been demonstrated, experimentally, to improve transistor performance by orders of magnitude without compromising other aspects of transistor action.[105]

4.4. Channel Passivation. The 2D material's channel passivation has similar issues as choosing the device's gate dielectric. In the case of TMDCs, chalcogen vacancies are introduced inadvertently during the CVD growth. These vacancies are therefore required to be passivated. For example, vacancy passivation of WSe_2 by incorporation of oxygen at the vacancy site[106] and MoS_2 by (3-mercaptopropyl) trimethoxysilane (MPS) grown on top[107] were reported recently. Similar vacancy healing mechanisms have been demonstrated via superacid TFSI and hydracids (HCl, HBr, HI) to enhance the PL intensity in monolayer TMDCs.[108−110] Treatment of MoS_2 with other sulfur-rich molecules like alkanethiol[111] and ammonium sulfide[112,113] have resulted in a significant reduction in the SV concentration, which has been validated by photoluminescence (PL), Raman, and device characterizations. PL and XPS results confirm a significant reduction in Se/S vacancies. Moreover, these techniques have resulted in significant improvements in electron conductivity and photoconductivity. Most of these methods, however, are not scalable to wafer-scale. Keeping this gap in mind, a sulfur-based technique to engineer a TMDC transistor channel has been demonstrated wherein a TMDC sample is kept inside a CVD chamber for H_2S exposure under certain conditions. This process of treating the channel with S species has led to defect passivation, subsequently validated by Raman, photoluminescence, and X-ray photoelectron spectroscopy data.[105] As a result, improved drain current modulation and gate control are observed in devices with the engineered channel (Figure 18). This has been attributed to the annihilation of traps and passivation of chalcogen vacancies present in the channel. Besides, reduced defect density and donor states have led to improved carrier mobility and normally OFF behavior, respectively (Figure 18). Most importantly, this technique turns out to be generic for all TMDCs, as depicted in Figure 18. Such an approach to engineer the channel is performed inside a CVD growth reactor, thereby making it an industrially feasible process.

4.5. Doping. Unlike bulk silicon, 2D materials are atomically thin, so implantation-based doping methods are not feasible in the case of 2D materials as it can potentially damage the film and change the intrinsic properties of the SC.[114] Doping 2D materials electrostatically is a noninvasive way to modulate carrier concentration in the FET channel and contact.[115] While it effectively improves contact properties, it is not feasible to use an additional gate terminal for increasing local carrier concentration. Typically, when doped via any surface charge transfer technique 2D TMDCs' dopant molecules are made to adsorb on the TMDC surface chemically.[114−123] Surface charge transfer doping for MoS_2 has been demonstrated earlier by using potassium metal,[116] benzyl viologen,[118] metal nanoparticles,[119] $Cs(CO)_3$,[120] metal ions,[121] and gold chloride solution.[117,122] The fundamental principle behind charge transfer doping is the electronegativity difference between TMDC atoms and dopant species. Depending on the relative electronegativity of dopant molecule with respect to that of TMDC molecule, the dopant acts either as a donor or an acceptor.[114] In most cases, such molecules degenerately dope the TMDC by transferring excess

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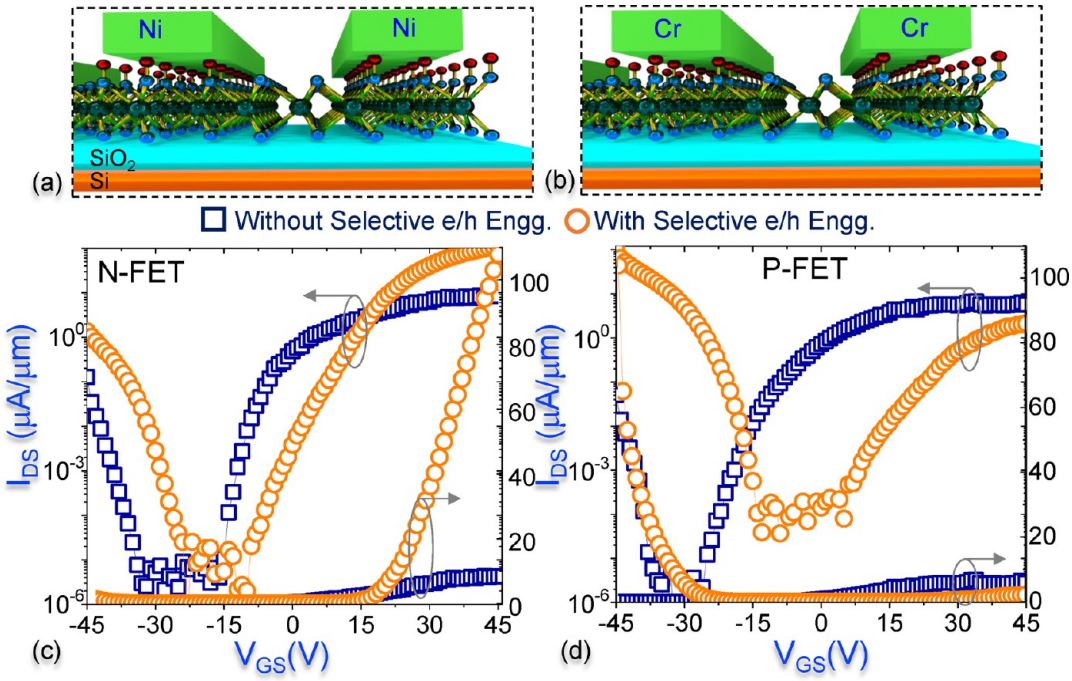

Figure 20. (a,b) WSe_2 channel-based n- and p-FET. Here selective n- and p-channel operation is achieved by engineering either electron or hole current injection by creating metal-induced (and chalcogen-assisted) midgap states in the WSe_2 under the contacts. (c,d) Input characteristics depicting selective n- and p-channel operation, respectively.[114]

electrons/holes and pull the Fermi level closer to the conduction band minimum (CBM)/valence band maximum (VBM). This results in a significant reduction in the SBH and enhanced thermionic injection of charge carriers. Surface charge transfer doping methods have resulted in a remarkable n- and p-type performance improvement of TMDC FETs. Among various surface charge transfer doping methods, KI doping of TMDCs, as depicted in Figure 19, is found to be relatively stable and cost-effective. It has resulted in a current density as large as 500 μA/μm without compromising on other figure of merit parameters and long-term material/device stability.[123] In general, doping techniques which require solvent-based chemical processes limit the process scalability and give rise to stability and/or reliability concerns in TMDC FETs. These issues can be addressed by high-k dielectric-based charge transfer doping using dielectrics like amorphous titanium oxide (ATO), magnesium oxide (MgO), Cs_2CO_3 (electron doping in BP), and MoO_3 (hole doping in BP).[124−128]

4.6. Selective p- and n-Channel Operations. The presence of chalcogen vacancy-induced midgap states in TMDCs leads to pinning the metal Fermi-level (FLP) closer to the conduction band.[106] As a result, TMDC transistors exhibit n-type (MoS_2 and WS_2) and ambipolar ($MoSe_2$ and WSe_2) conduction. The ambipolar behavior in $MoSe_2$ and WSe_2 transistors involving dominant electron conduction through the device for FLP occurs at lower energy, however, still closer to the conduction band than valence band.[129] This implies that establishing hole current through TMDCs is not trivial. However, in order to have 2D TMDC-based electronic integrated circuits, realizing transistors with opposite polarity is imperative. The use of high work function material like MoOx as an interlayer between TMDC and metal has proven effective in suppressing FLP.[130] This enabled hole conduction across an otherwise n-type MoS_2 transistor as demonstrated by Steven et al.[130] Use of surface dopants like NO_2[131] and $AuCl_3$[132] at the contacts is another way of realizing high-performance p-type conduction in TMDCs. However, the air stability of NO_2 and large Schottky barrier at the $AuCl_3$-doped MoS_2/Pd contact limit the transistors' performance to dope via such surface charge transfer doping methods. Besides using dopants with an additional charge to dope the channel and/or contact, functionalized substrate-induced doping has been performed where fluoroalkyltrichlorosilane self-aligned monolayer (SAM)[133] is used to functionalize the substrate dielectric and induce hole doping in TMDCs.[134] The use of SAM reduces interfacial impurity scattering, thereby improving carrier transport in the channel. Substitutional doping by Nb of MoS_2[135] during growth, high-energy phosphorus implantation,[136] and intentionally growing transition metal deficient TMDCs are other methods to realize inherently p-type TMDCs. Recently, sulfur-based contact engineering has been reported to selectively control the polarity of WSe_2-based FETs (Figure 20a,b). Samples were exposed to H_2S inside a CVD chamber under certain conditions, suitable for the decomposition of H_2S, followed by contact metal deposition. It was observed that contact engineered WSe_2/Ni devices exhibit enhanced n-type performance (Figure 20c), whereas contact engineered WSe_2/Cr devices exhibit p-type conduction (Figure 20d), comparable to the n-type current observed in Ni contacted devices. Fundamental insights were developed, which revealed that S interstitial impurities, introduced by H_2S-based contact engineering, behave differently in the presence of Cr than they do when Ni is at the surface. The technique is essentially used to engineer the location of FLP closer to the VBM in the presence of Cr, thereby facilitating hole conduction and reducing TB for Ni contacted devices to enhance already persisting n-type conduction. Such a process is promising for enabling CMOS operation using TMDCs.[137]

4.7. PR Residue and Unintended Doping Free Patterning. Physical and chemical residue to photoresist

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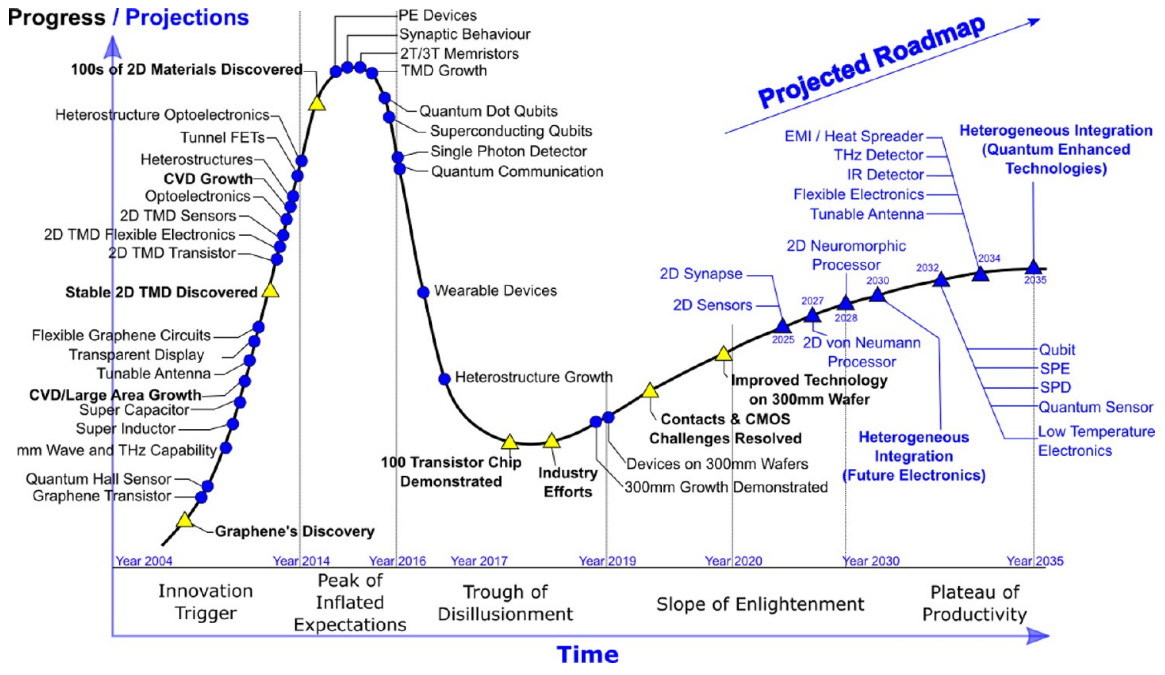

Figure 21. A projected roadmap for 2D materials and 2D material-based technology enablement.

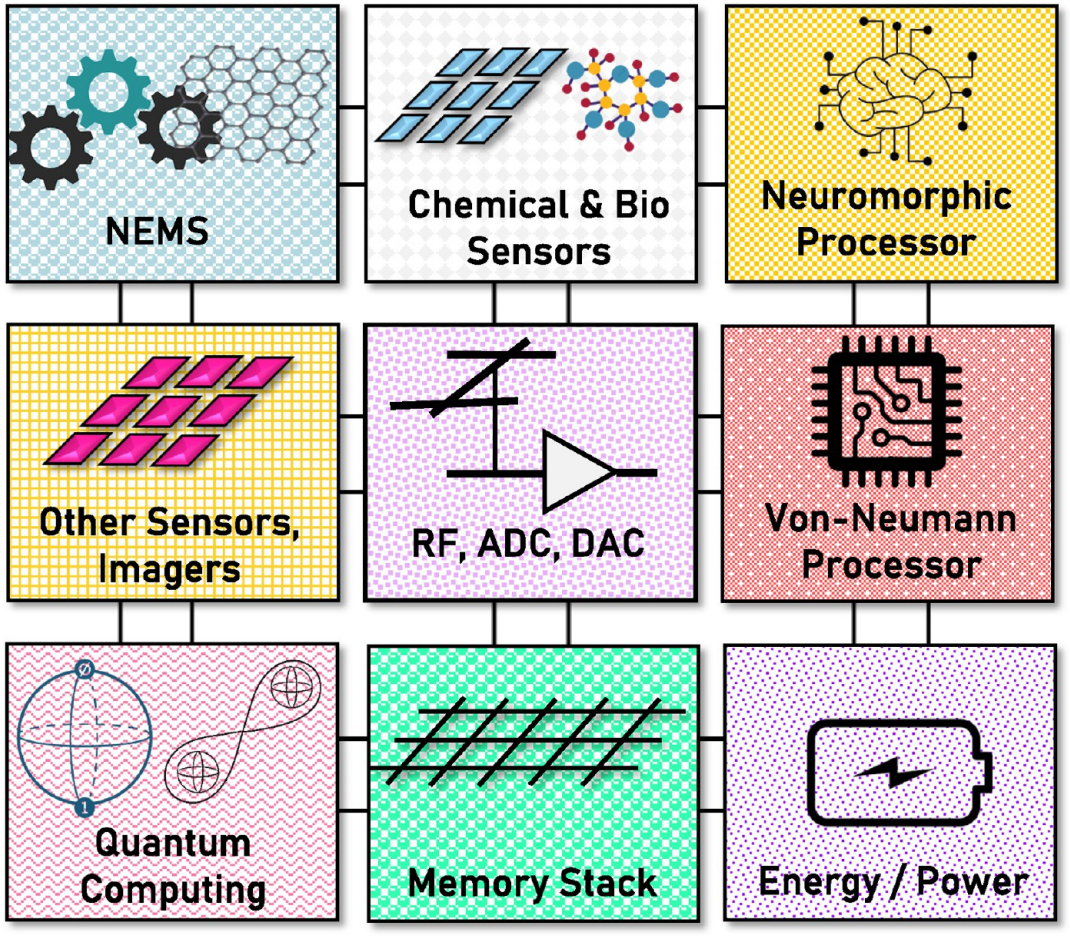

Figure 22. Projected possibility and ability of 2D material-based universal technology platform to enable heterogeneous integration of future electronics, optoelectronics, and quantum enhanced technologies.

post-plasma/patterning process is a pivotal issue to be addressed in the case of 2D materials. Patterning or plasma etching of 2D layer is required to define a given layer/2D material's active region. However, when exposed to plasma processes while

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keeping the active region covered by photoresist, these materials lead to the physical residue of photoresists (post-acetone/IPA cleaning) over the 2D material surface. In graphene, this aspect is attributed to a strong chemical bonding between graphene and PR material through its interaction with graphene out-plane π-orbitals. It can also lead to unintentional chemical doping of the graphene/TMDC channel, increasing the OFF-state leakage and decreasing the ON-state current. These aspects require serious attention while developing a wafer-scale 2D material-based process.

4.8. Large Scale Integration. The very first 2D material-based integrated circuit, which was a graphene FET-based RF mixer capable of operating at 10 MHz, was demonstrated by Wang et al. in 2010[138] and the same with improved performance by Lin et al. in the year 2011.[139] Radisavljevic et al. demonstrated logic operation[140] and amplifier[141] using MoS_2 channel-based devices. Wang et al. demonstrated large-area circuits, that is, basic building blocks for logic and analog operations, using MoS_2 channel FETs.[142,143] Kim et al.[144] and Cheng et al.[145] demonstrated the usability of 2D material for flexible electronics and MoS_2-based high-speed circuits on flexible substrates, respectively. Subsequently, Sanne et al. demonstrated large-scale integration by demonstrating RF amplifiers and other circuits using CVD MoS_2.[146] Das et al., Tosun et al., Yu et al. and and Zhu et al. demonstrated logic circuits using WSe_2 FETs[147−150] and AM demodulator using phosphorene FETs.[150] Gajarushi, A. S. et al. demonstrated logic inverters using graphene FETs.[151] The large-scale integration of 2D MoS_2 FETs was demonstrated recently by Wachter et al. by demonstrating a 1 Bit microprocessor.[152] So far, this work has demonstrated the most complex circuit integration using 2D materials while using 115 transistors in a single chip.

4.9. Long-Term Reliability. The reliability of 2D material-based devices is also an emerging challenge that requires dedicated efforts and explorations to address it. The degradation and failure physics is found to be very different than conventional materials like Si or Ge. For example, graphene devices fail due to significant electron−phonon scattering at the grain boundaries, which increases the phonon population and results in the chemical breakdown of graphene lattice near grain boundaries.[153,154] MoS_2, on the other hand, undergoes material reconfiguration under the application of long-term electrical stress, which is unique to TMDCs.[155,156] Phosphorene behaves differently, as it undergoes chemical breakdown when exposed to ambient conditions.[157,158]

5. ROADMAP: HETEROGENEOUS INTEGRATION WITH 2D MATERIALS

The end of Moore's law and the emergence of beyond-Si electronics, optoelectronics, and quantum technologies are well-accepted directions of the past decade. Heterogeneous integration of various functionalities, including sensing, neuromorphic, optoelectronics, and quantum technologies, is projected to be the driving force for industries in the coming decades. This has pushed stakeholders to think of universal technology platforms and better ways to meet the needs of future application. Keeping in mind the promises of 2D materials and various applications to which it can cater, as discussed in the previous section, a 2D material-based technology platform has the potential to offer heterogeneous integration capability. Worldwide efforts using 2D materials though cover the entire spectrum from beyond-Si electronics to quantum technologies (see Figure 21, Years 2004−2015), the approach followed until recently has been disconnected. From an industry perspective, a universal platform would be the most efficient and cost-effective way to enable heterogeneous integration. Keeping this in mind, the industry has started putting efforts in this direction (see Figure 21, Years 2017−2020). Figure 22 depicts a projected heterogeneously integrated system expected to be enabled by a universal 2D material technology platform. This would require dedicated science and engineering efforts to enable various technology modules such as (i) crossbar integration of synapses and sensors, (ii) von Neumann and neuromorphic processors, (iii) optoelectronics, (iv) quantum devices, and (v) low-temperature electronics using 2D materials, as projected in Figure 21.

Maturing 2D technology for meeting this roadmap and enabling heterogeneous integration also brings several/unique challenges, which are worth highlighting despite the promise that 2D materials offer for a plethora of applications. Large scale single crystal (or large grain size) growth of TMDC is a challenging task and requires dedicated efforts. This is one of the key reasons why 2D TMDC FETs, realized over CVD growth material often underperform when compared to Si MOSFETs. The same however outperform at the lab scale when single crystal material (using exfoliation) is used. Although monolayer growth is sufficient for optoelectronic, sensing, neuromorphic and quantum applications, for logic and memory applications a layered growth is highly desirable. This requires additional level of optimization. In the case of graphene, the growth is relatively mature, which results in performance close to theoretical limits. On the other hand, the lithography process free from photoresist residues and resulting damage has been addressed at the laboratory level and is still a challenge for both graphene and 2D TMDCs in the case of wafer scale process. Contacts to 2D TMDCs and graphene were earlier considered to be a fundamental limiting factor, which were recently addressed using atomic overlap engineering that brings wafer scalable approaches to lower the contact resistance down to fundamental limits. Gate dielectric for these materials is a nontrivial matter due to lack of native oxides of 2D materials. This also makes the gate oxide reliability in 2D devices a topic of concern. Therefore, gate stack development for graphene and 2D TMDCs, while keeping in mind long-term gate oxide reliability, requires focused efforts. One would need to develop comprehensive device models with built-in process irregularities and material defects to enable design of heterogeneous technologies. Dedicated efforts in terms of large-scale integration of 2D devices and heterogeneous integration of 2D applications are also required. These threads are expected to grow in the next 15 years, eventually leading to a universal 2D material technology platform for heterogeneous integration of quantum-enhanced technologies by 2035, as projected in Figure 21.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.1c00729.

Electrical and thermal properties of various 2D materials (Table S1), optical properties of various 2D materials (Table S2) (PDF)

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Notes

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