ESD Behavior of AlGaN/GaN HEMT on Si: Physical Insights, Design Aspects, Cumulative Degradation and Failure Analysis

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***Abstract*—This experimental study reports ESD failure analysis of AlGaN/GaN HEMTs. Effect of MESA isolation, gate and parasitic MESA Schottky diode on ESD robustness is studied. Cause of snapback instability, multiple NDCs and transition from soft-to-hard failure are discussed. Unique leakage trends and cumulative nature of degradation are discovered. Post failure analysis reveals role of inverse piezoelectric effect, fringing electric field, contact resistivity, temperature and field induced contact metal migration in degradation of AlGaN/GaN HEMTs under ESD conditions.**

1. Introduction

Gallium Nitride (GaN) has emerged as a promising material for high power and high frequency applications. The impressive properties of GaN like wide bandgap (3.4 eV), high breakdown field (3.3 MV/cm) and low dielectric constant (9) make it an attractive material option over Si for high power applications. The strong spontaneous and piezo-electric fields, 3 MV/cm and 2 MV/cm [1], respectively, which are intrinsic to AlGaN/GaN material system, give rise to high 2D electron gas (2DEG) density (10^{13} cm^{-2}) at the AlGaN/GaN hetero-junction. Moreover, the 2D confinement enhances the carrier mobility (1500-2000 cm^{-2}/V) which results in high electron peak velocity (3×10^7 cm/s) and saturation velocity (1.5×10^7 cm/s) making AlGaN/GaN HEMT (High Electron Mobility Transistor) attractive for the RF applications also.

Although the cost of AlGaN/GaN HEMT has significantly reduced in recent years, due to its growth over conventional Si, reliability poses a great challenge to its widespread use. The long term reliability of AlGaN/GaN HEMT is widely discussed in the literature, however very limited discussion is available on its ESD (Electrostatic Discharge) reliability [2-7] and needs further investigation.

This work reports nature and type of ESD failure in AlGaN/GaN HEMT stressed under different ESD conditions and is summarized in five sections. Section-2 covers the device fabrication details and the device geometries used in this study. Measurement set-up and ESD stress conditions used are described in Section-3 and 4 respectively. Moreover, relation between device degradation and failure, cumulative nature of degradation, transition from soft to hard failure, cause of snapback instability and multiple NDC (Negative Differential Conductance) regions in HEMT, are discussed in Section-5 together with investigation of impact of various design aspects like MESA isolation, gate and surface passivation on ESD behavior of AlGaN/GaN HEMT.

2. Device under Investigation

AlGaN/GaN HEMT stack as shown in Fig. 1a, was grown using MOCVD (Metal Organic Chemical Vapour Deposition) on a 2-inch Silicon (111) substrate. Normally-ON HEMTs of 100 μm device width and (i) w/ and w/o gate, (ii) w/ and w/o MESA isolation were processed using UV lithography. MESA isolation was achieved using Chlorine based Inductively Coupled Plasma-RIE (Reactive Ion Etching). Ti/Al/Ni/Au metal stack was sputter deposited using E-beam evaporation and later annealed at $\sim$ 850 °C temperature to realize Ohmic contacts. Finally, Ni/Au based Schottky gate was deposited, followed by a low temperature anneal. Surface passivation was ignored in these devices to avoid its impact, if any, on the ESD behavior. SEM (Scanning Electron Microscopy) micrograph in Fig. 1b shows the top view of one of the fabricated devices.

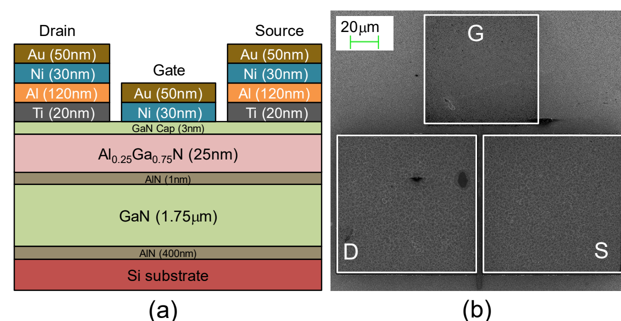

Figure 1. (a) Schematic view of processed device depicting stack of various layers grown for AlGaN/GaN HEMTs; and (b) SEM micrograph / top view of the fabricated device shows the gate, source and drain pads with gate finger in between. Devices under stress are HEMTs w/ & w/o gate and w/ & w/o MESA with different source-to-drain spacing (L_{SD}) under grounded gate and floating gate conditions

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3. Measurement Techniques

ESD pulses of varying pulse width (PW) and fixed rise time (1 ns,) generated using a TLP tester (HPPI), were used to investigate ESD behavior of HEMT. Voltage and current waveforms, recorded using a DSO (Digital Storage Oscilloscope), were averaged over 60 ns-90 ns time interval to obtain I-V characteristic of the device under test. After each pulse, device was characterized for its DC behavior and linear drain current (I_{DS}) was measured at low drain bias (V_{DS} = 50 mV), to monitor device degradation and failure. On-the-fly monitoring of device was done to observe evolution of device failure, using a high resolution microscope (Motic PSM-1000) with 400× optical zoom and high speed integrated CCD camera. Figure 2 shows the schematic of the measurement set-up. All the measurements were carried out at room temperature (25 °C).

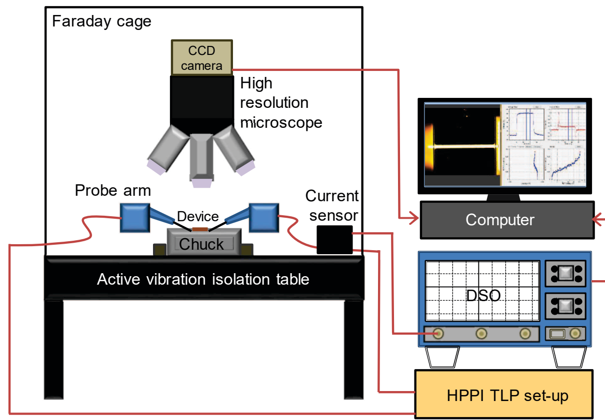

Figure 2. Characterization setup used for ESD analysis of AlGaN/GaN HEMTs.

4. TLP Characterization

TLP characteristics of HEMT with different device geometries viz. (i) without gate and MESA isolation, (ii) without gate and with MESA isolation, (iii) with gate and MESA isolation, with varying source-to-drain spacing (L_{SD}) are shown in Fig3. Devices were characterized under different gate bias conditions at various TLP pulse widths (PW). In all cases, linear TLP characteristics are observed, at low voltages, due to normally-ON nature of the device. However, at higher voltages a unique snapback characteristic is observed, on the verge of avalanche breakdown, in each case. Moreover, post snapback holding state is missing in most of the cases and the device failed immediately after few ESD pulses in the snapback regime. In all the cases, snapback voltage (V_{SNAP}) increased with increase in source-to-drain spacing (L_{SD}) due to reduced electric field in the channel. Also, the ON-resistance (R_{ON}) was found to increase and V_{SNAP} interestingly falls with an increase of PW. This is attributed to rise in self heating at higher PW. Degradation in linear drain current was also observed from spot measurements, which is discussed in the next section.

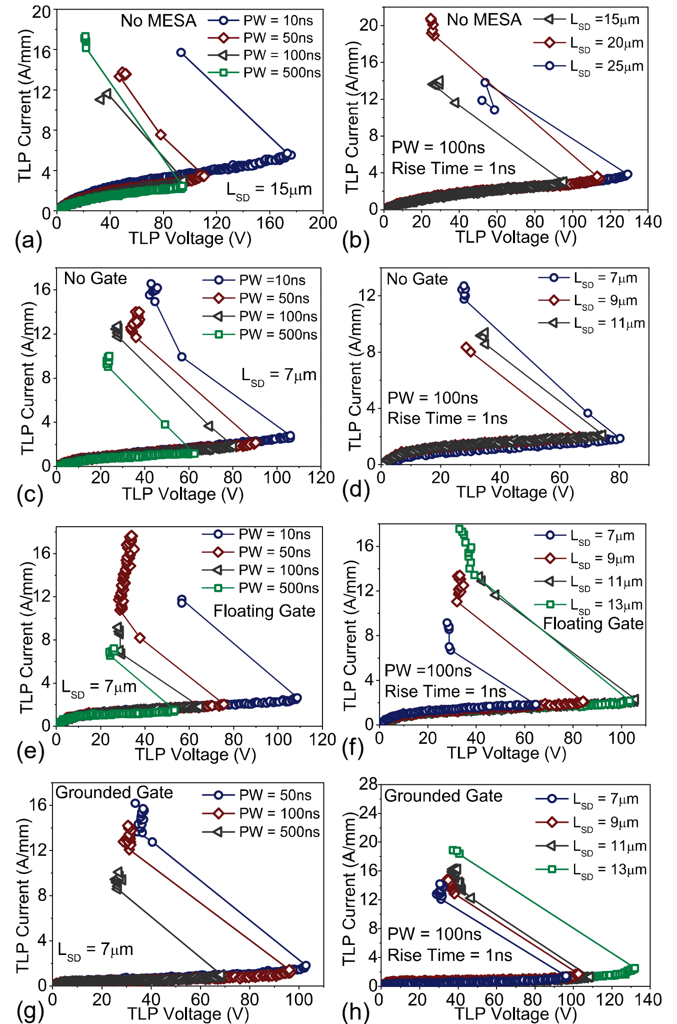

Figure 3. TLP characteristics at different (i) pulse width and (ii) L_{SD} for AlGaN/GaN HEMT (a-b) without gate and MESA, (c-d) without gate and with MESA, (e-f) with floating gate, (g-h) with grounded gate. Figure shows (i) decrease in V_{SNAP} and increase in R_{ON} with increase in PW due to increased self heating and (ii) improvement in V_{SNAP} with increase in L_{SD} at fixed PW = 100ns due to reduced lateral field.

5. Analysis and Discussion

5.1. Effect of MESA on ESD Robustness

The device configuration without MESA sees an early ESD failure compared to MESA isolated test structure. The post failure SEM micrograph of the device without MESA shows prominent metal migration from the contact edges under the influence of high fringing electric field (Fig. 10a). High current level during ESD raise the lattice temperature and cause significant heating in S/D (Source/Drain) contacts

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which can melt the contact metal. Moreover, in the absence of surface passivation metal migration gets further enhanced due to thermal diffusion of metals via surface defects. Therefore, device fails at low ESD stress in absence of MESA and passivation.

When device with MESA, is stressed under same ESD condition, the migration is observed to be confined to the channel region and does not occur at contact corners (Fig. 10b-Fig. 10d). This can be explained as follows; in MESA isolated device, AlGaN layer is absent near contact corners. Therefore migration from contact corners, via AlGaN surface states, is not possible. However, at higher stress voltage, presence of strong electric field within the channel region assists electromigration between the device S/D contacts and causes device failure.

5.2. Effect of Gate on ESD Robustness

The influence of gate and its vertical field on ESD robustness of HEMT, is studied by comparative analysis of behavior of HEMT with and without gate electrode, under same ESD condition (100 ns). In HEMT without gate, lower snapback voltage is obtained compared to that in gated device as shown in Fig. 4. This can be attributed to modified electric field profile in the channel region in presence of Schottky gate which forms a depletion region close to channel. To gain further insight into the effect, a HEMT test structure with partially gated channel region is stressed under 50 ns stress. Post failure SEM micrograph (Fig. 10e) of the device, reveals that degradation preferably occurs in the non-gated region which shows that absence of gate makes the device more vulnerable to ESD failure. SEM micrograph shows that the failure occurred due to migration of metal from the edge of Ti/Al/Ni/Au drain stack to source. EDX (Energy Dispersive X-Ray) analysis of the shorted region confirms Al (6 %) which migrated from drain contact. Furthermore, in gated devices, floating gate configuration is found to be more susceptible to ESD event than grounded gate, as seen in Fig. 4. This is because of the capacitive coupling between drain and gate which induces voltage on otherwise floating gate. The induced gate voltage increases linearly with drain voltage till it equals cut-in voltage of gate-to-source (GS)Schottky diode and results in unwanted turn-ON of GS Schottky diode, followed by its degradation and subsequent device failure [5].

5.3. Effect of Pulse Width on ESD Robustness

TLP characterization of various device configurations at different pulse width (PW) (Fig. 3) shows that ESD robustness of the device decreases with increase in PW, which is attributed to the enhanced self heating across the device and the associated degradation. Comparison of SEM micrographs (Fig. 10b - Fig. 10d) of the devices highlights that device degradation accelerates, due to enhancement in metal migration rate, at higher PWs. Hence, device sees early ESD failure at higher PW.

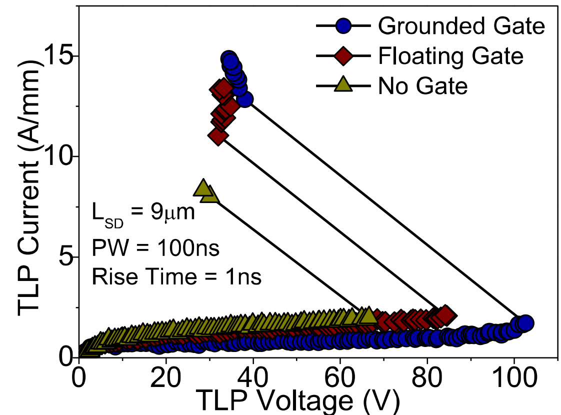

Figure 4. Comparison of TLP characteristics of AlGaN/GaN HEMTs with and w/o gate.

5.4. Device Instabilities in Snapback Region

At lower ESD stress power, the device behavior in the snapback region is found to be unstable. For example, when device without MESA (L_{SD} = 7 μm) and device with floating gate (L_{SD} = 15 μm), when stressed at PW = 10 ns, device behavior oscillates between normal and snapback regime as shown in Fig. 5a. Also, multiple negative differential conductance (NDC) regions ie. NDR-1 and NDR-2, are observed under the grounded gate mode as in Fig. 5b. Post failure SEM images of the corresponding devices show multiple damages along the gate finger (Fig. 10f), which confirms that multiple sections of the device width independently trigger into snapback. Figure 6 depicts the comparison of device voltage waveform, recorded around snapback point, in HEMT (L_{SD} = 15 μm) stressed at different pulse widths. It reveals that as the pulse width increases the device failure mode changes from soft to hard. Clearly, due to low self heating at low pulse width ie. 10 ns, degradation occurs softly and is not significant to cause deep snapback and abrupt device failure. However, as the pulse width increases, the device instabilities vanish and results in catastrophic failure of the device (Fig. 10g - 10h) triggered by development of cracks under the gate.

5.5. Unique Leakage Trends

Linear drain current (I_{DC}), measured after each stress pulse, exhibits a unique degradation trend with increasing stress level, for each device configuration under stress as depicted from Fig.7a. Different degradation trends point towards different failure mode in each case eg. in absence of MESA, metal migration from contact corners, gradually reduces the S/D spacing which is reflected as continuous increase in I_{DC} whereas under floating gate stress, channel continuously degrades leading to decrease in I_{DC}. HEMT with grounded-gate sees maximum change (28%) followed by HEMT without gate (22%), with floating-gate (17%) and without MESA (5%), in I_{DC}.

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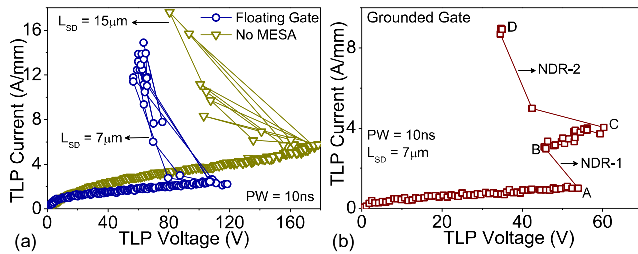

Figure 5. Instability in snapback region at 10ns ESD stress (a) in case of HEMT without MESA isolation and HEMT stressed under floating gate condition. Device oscillates between normal and snapback regime. (b) Multiple negative differential conductance regions (NDC- 1, NDC-2) are observed in HEMT ESD stressed at drain with 10ns pulse under gate grounded condition.

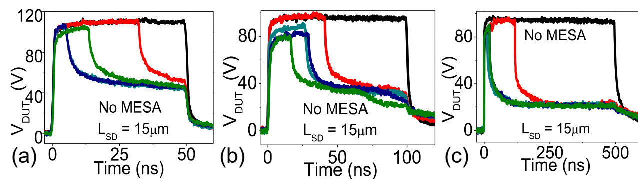

Figure 6. Evolution of voltage waveform across the device without MESA at snapback point for different pulse widths. The device failure changes from soft to hard with increase in pulse width.

5.6. Cumulative Nature of Degradation

To further study the type of degradation and its nature,device is stressed using a set of ten consecutive ESD pulses (100 ns) of fixed amplitude under floating gate condition. Subsequently, the pulse amplitude was increased to higher voltage and linear drain current (I_{DC}) is measured after each set. Fig. 8 shows gradual degradation in the drain current with increase in number of pulses of fixed amplitude. Moreover, it shows that repeated stress leads to accumulative degradation, which reduces the snapback voltage and leads

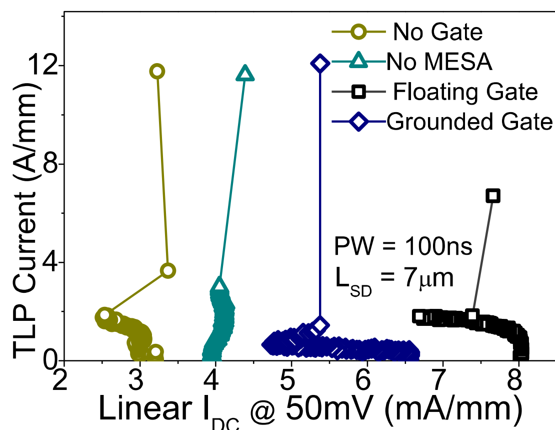

Figure 7. Unique degradation trend in linear drain current of AlGaN/GaN HEMTs with and w/o gate and MESA isolation when stressed with 100ns ESD pulse at the drain.

to early device failure. This cumulative nature of degradation can be attributed to trap generation and carrier trapping in various regions of the device or development of crack and metal migration after each pulse. The later is depicted in Fig. 9 which shows the device under stress at different instants of time.

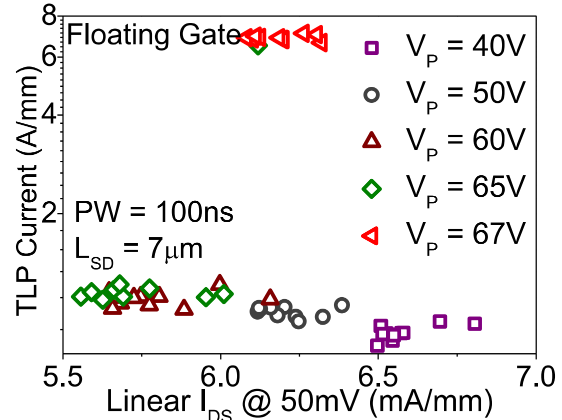

Figure 8. Decrease in linear drain current (I_{DC}) with each pulse when the device is stressed with ten similar consecutive pulses. The pulse amplitude (V_P) is increased in consecutive sets. Device exhibits snapback even for V_P less than V_{SNAP} due to cumulative degradation.

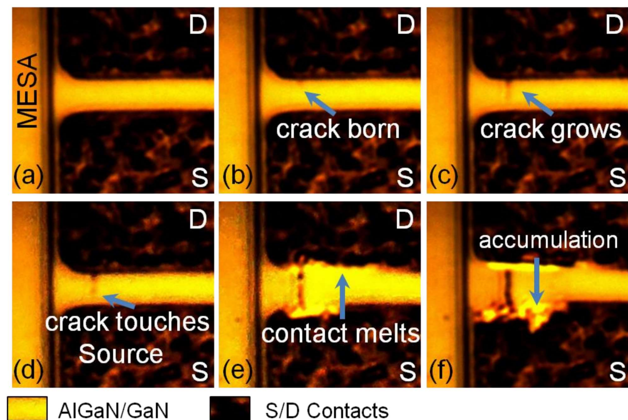

Figure 9. A sequence of events captured during 50ns ESD stress on drain of HEMT without gate and with MESA. The microscope settings are adjusted for high contrast for improved visibility.

6. Conclusion

Different degradation phenomena were observed to be responsible for failure of AlGaN/GaN HEMT, under different ESD conditions which reflected in unique trends shown in linear drain current degradation. Linear drain current was observed as a strong signature of type and amount of degradation in AlGaN/GaN HEMT. Cumulative nature of degradation was discovered and observed to fail HEMT even at much lower ESD stress level. Unstable device behavior

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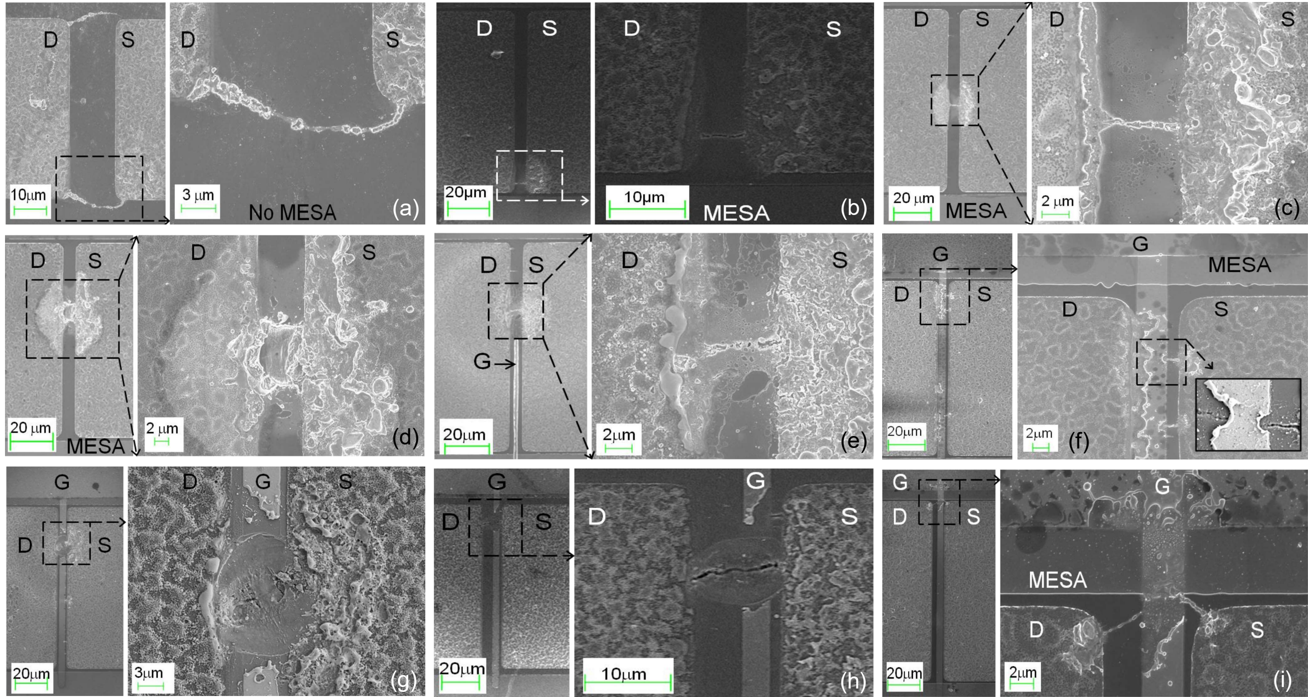

Figure 10. Post failure SEM micrograph of different device configurations depicting different failure modes. (a) HEMT device without MESA and gate after 50ns ESD stress. Figure shows the curved short paths between drain and source formed due to metal migration under fringing electric field. EDX analysis of short portion confirms Ni (7.27%) which melted and migrated from the Ti/Al/Ni/Au drain contact stack. (b) HEMT device with MESA and without gate after 50ns ESD stress on drain, showing crack developed due to inverse piezoelectric effect. (c) HEMT device with MESA and without gate after 100ns ESD stress on drain. Figure shows a source-drain short formed within in the channel region. EDX analysis of short portion confirms Al (8.7%) which melted and migrated from the Ti/Al/Ni/Au drain contact stack. (d) HEMT device with MESA and without gate after 500ns ESD stress on drain, showing increased migration at higher pulse width (500ns). (e) Partially gated HEMT after 50ns ESD stress, showing device failure preferably occurred in ungated region. (f) HEMT after 10ns grounded gate ESD stress. Figure shows damaged gate finger with crack underneath. (g) HEMT after 50ns grounded gate ESD stress. Figure shows gate finger blown-off at a dislocation site. (h) HEMT after 100ns grounded gate ESD stress. Figure shows a crack between drain and source with damaged gate finger. (i) HEMT after 100ns ESD stress between gate and drain (source floating) showing failure due to premature breakdown of parasitic MESA Schottky resulting in gate to S/D short and metal removal from the gate pad. diode.

was observed in snapback regime at smaller pulse width and vanished at higher pulse width. Device design aspects like MESA isolation and gate showed significant impact on ESD robustness of AlGaN/GaN HEMTs. Parasitics like MESA Schottky diode deteriorated the ESD robustness and should be taken care in ESD robust HEMT design.

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