On the ESD Behavior of AlGaN/GaN Schottky Diodes and Trap Assisted Failure Mechanism

Bhawani Shankar (1), Rudrarup Sengupta (1), Sayak Dutta Gupta (1), Ankit Soni (1), Nagaboopathy Mohan (2), Navakanta Bhat (2), Srinivasan Raghavan (2) and Mayank Shrivastava (1)

(1) Advance Nanoelectronic Device and Circuit Research Laboratory, Department of Electronic Systems Engineering, Bangalore, 560012, India, tel.: +91-80-2293-2732, e-mail: bhawanishankar@dese.iisc.ernet.in

(2) Center for Nanoscience and Engineering, Indian Institute of Science, Bangalore, 560012, India

Abstract – This experimental study reports ESD behavior of novel designs of GaN Schottky diodes. Impact of electro-thermal transport, device degradation and trap generation on its ESD robustness is analyzed. Role of interface traps in ESD failure of GaN Schottky diode is investigated. Transition from soft-to-hard failure, which is found to depend on diode area, presence of traps and diode design is discussed. Unique degradation trends, cumulative nature of degradation and trap assisted failure modes are discovered.

I. Introduction

Gallium Nitride (GaN) has emerged as a promising alternative for Si or SiC based power devices, thanks to its wider bandgap (3.4 eV), high breakdown field (3.3 MV/cm) and low dielectric constant (9). The strong spontaneous and piezoelectric fields, 3 MV/cm and 2 MV/cm, respectively, which are intrinsic to AlGaN/GaN material system, give rise to high 2D electron gas (2DEG) density (~10^{13} cm^{-2}) at the AlGaN/GaN hetero-junction. The 2D confinement enhances the carrier mobility (1500-2000 cm^2/V) which results in high electron peak velocity ($3x10^7$ cm/s) and saturation velocity (1.5 x 10^7 cm/s) making AlGaN/GaN heterojunction attractive for the high frequency and fast switching applications. Along with transistors, diodes too are indispensable elements in a power electronic circuit. Si MOSFET has a body diode, which offers reverse protection. However, the same is absent in AlGaN/GaN HEMT. In addition to this, for a complete GaN based power electronic circuit design, GaN based diodes are in great demand. Keeping this in mind, GaN Schottky diode has attracted attention as it offers monolithic integration with GaN HEMT [1] – [3]. Limited discussion on long term reliability of GaN Schottky diode is present in the literature [4] – [5]; however, the same on ESD or high current reliability is missing. With this as a motivation, in this work we, for the first time, report high current reliability of AlGaN/GaN Schottky diodes. Beside current transport, turn-on behavior and device degradation, role of interface traps in device failure is revealed.

II. Device under Test

Two types of AlGaN/GaN Schottky diodes; (i) without recessed Schottky (Anode) contact, where Schottky contact is placed on GaN cap layer of AlGaN/GaN stack, offering vertical conduction and (ii) with recessed Schottky (Anode) contact, where Schottky contact is placed next to 2DEG, which offers lateral conduction (Fig. 1). Schottky contact is formed on GaN cap rather than directly on AlGaN/GaN, because GaN capping layer offers low surface roughness and is observed to improve Schottky barrier height in AlGaN/GaN HEMTs [6]. Schottky barrier with low surface roughness and higher barrier height makes the Schottky interface more ESD robust because of following reasons; (i) Low surface roughness leads to lower interface roughness and uniform barrier height across the Schottky junction which helps in uniform current conduction through the Schottky contact. (ii) Furthermore, smaller interface roughness leads to lower interface states density (Dit)/ traps and suppressed interface scattering of carriers. (iii) Also, higher Schottky barrier height suppresses the leakage current. The cathode contact was always ohmic in nature. Before realizing test structures, device design studies, using (i) recess depth (ii) Schottky barrier height and (iii) anode-to-cathode spacing were performed for an optimum design. Figure 2 shows DC I-V characteristics of fabricated GaN Schottky diodes. Attributed to side wall conduction, Schottky diode offers 4x lower cut-in voltage and 6× higher current compared to the device with vertical conduction (without recess).

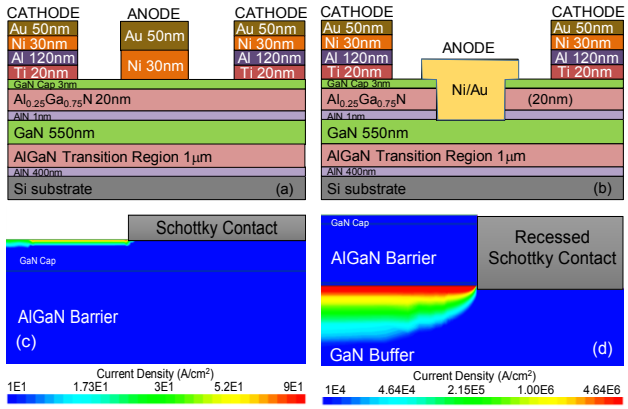

Figure 1: Schematic view of AlGaN/GaN diodes under test (a) without recessed Schottky contact and (b) with recessed Schottky contact, depicting stack of various layers grown on Si. (c) Current density distribution in non-recessed diode and (d) recessed diode extracted using TCAD simulations. At 2V forward bias as depicted, current conduction in recessed diode is orders of magnitude higher than non-recessed diode, which is due to side wall conduction through Schottky contact.

For device fabrication, AlGaN/GaN material stack was grown using MOCVD on a 2-inch Si (111) substrate. Devices were MESA isolated by etching 180 nm GaN using Cl_2/BCl_3 chemistry in Inductively Coupled Plasma-RIE system. Ohmic contact (Cathode) was realized by depositing Ti/Al/Ni/Au metal stack followed by a high temperature (850 °C) anneal cycle. Recess was created by O_2/BCl_3 based atomic layer etching in RIE system. Ni/Au based Schottky (Anode) contact was deposited in the end, followed by a low temperature annealing in forming gas.

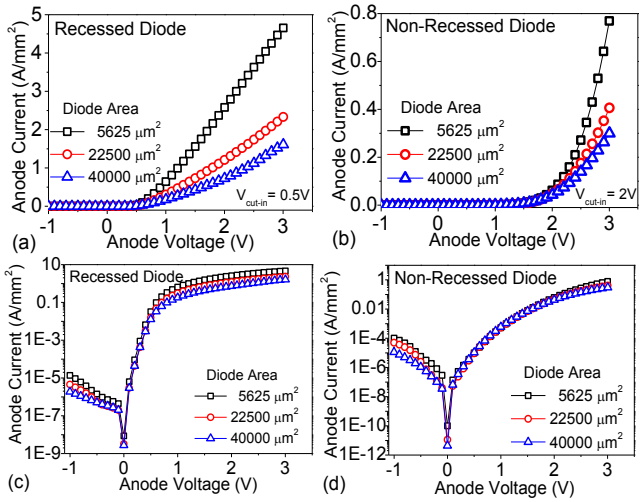

Figure 2: DC I-V characteristics of (a) Recessed and (b) Non-Recessed Schottky diodes. Figure shows (i) higher current density in case of smaller Anode area diode, which confirms side wall conduction and (ii) lower cut-in voltage of recessed diode compared to non-recessed diode, which results in 6× higher I_{ON} compared to non-recessed structure and (iv) higher I_{ON}/I_{OFF} ratio for (c) recessed structures than (c) non-recessed diode.

III. Measurement Technique

TLP behavior of GaN Schottky diodes was investigated using pulses with different pulse width (PW), however at fixed rise time (1 ns). Device voltage and current waveforms were averaged over 60% -90% of the pulse width. Anode current was spot measured under forward mode (@10 mV DC) to monitor device degradation and failure. Here, low DC bias was used to avoid device degradation during spot measurement. Moreover, devices were measured in the presence and absence of UV (365 nm) light to investigate the role of surface/or buffer traps. On the fly C-V measurements were performed during the test to monitor the evolution of interface trap density with stress. Capacitance was measured under reverse bias condition (-2 V) at low frequency (@ 20 KHz) and interface trap density (Dit) was obtained using the following relation [7];

$$Dit \approx \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{\max}$$

All the measurements were done at room temperature.

IV. Experiments and Observations

Schottky diodes with different anode area were stressed at the Anode, while keeping Cathode grounded, using pulses with different pulse widths. It is worth highlighting that presence of traps and carrier trapping at Schottky interface is often a serious reliability concern. Given that UV (365 nm) light assists in de-trapping majority of the traps present within the GaN bandgap, devices were stressed both under dark and UV conditions to monitor role of traps, if any, in the TLP I-V characteristics and high current transport. Figure 3-5 shows the TLP characteristics of recessed and non-recessed diode with different Anode area captured under dark and UV conditions, for different pulse width. At low voltages, recessed diode exhibits linear TLP characteristics however; non-recessed diode sees an initial pinch-off region before it turns-on. This is attributed to higher cut-in voltage (V_{CUT-IN}) of the non-recessed diode. At higher voltage the diode current saturates, which is limited by carrier density and defect states and saturation velocity in 2DEG. Depending on the device type or stress condition, which is discussed in detail below, device enters into a snapback state and immediate failure. Spot measurements, which are later complemented by C-V based trap investigation after uniform intervals of stress pulses, shows an interesting degradation trends. In all the cases, device was found to degrade

(increased diode leakage current) significantly, before it enters in a snapback state. Individual cases and comparisons are presented below.

A. Effect of Pulse Width

In all cases (Fig. 3 and 4) snapback voltage (V_{SNAP}) and failure current (I_{FAIL}) falls when pulse width was increased, which can be attributed to enhanced self-heating or higher (accumulative) degradation of Schottky interface. On one hand, forward current under linear region did not change at longer pulse widths, which however was found to lower under saturation condition. This confirms role of lattice heating at higher voltages. The drop was found to be significant in case of diode with recess. Longer pulses show hard breakdown, whereas shorter pulses lead to a pulse to pulse instability close to snapback point, which points to multiple localized failure regions. Finally, diode without recess faces a gradual degradation, whereas the same in case of recessed diode was abrupt in nature.

B. Effect of UV Exposure

Figure 4 shows an increased saturation current, unchanged failure voltage and lower on-resistance in presence of UV exposure. In addition to this, the device degradation was found to be more gradual rather the case before. This point to trap limited current conduction, current driven trap creation and trap assisted device degradation / failure.

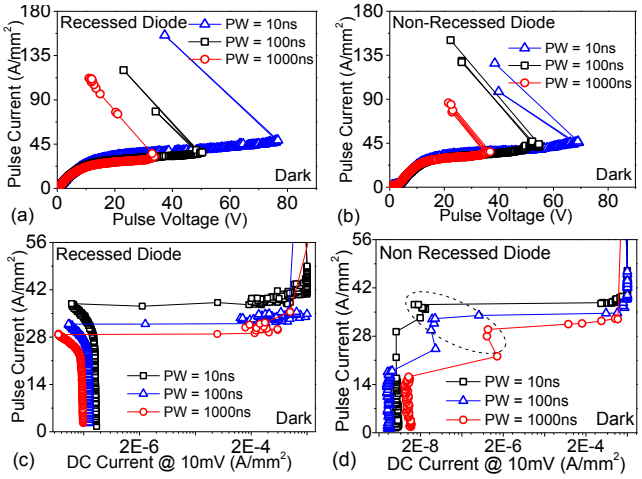

Figure 3: TLP characteristics of (a) recessed diode (b) non-recessed diode measured at different pulse width under dark condition. Degradation in spot measured DC current of (c) recessed diode and (d) non-recessed diode exhibiting abrupt degradation and soft / gradual degradation, respectively.

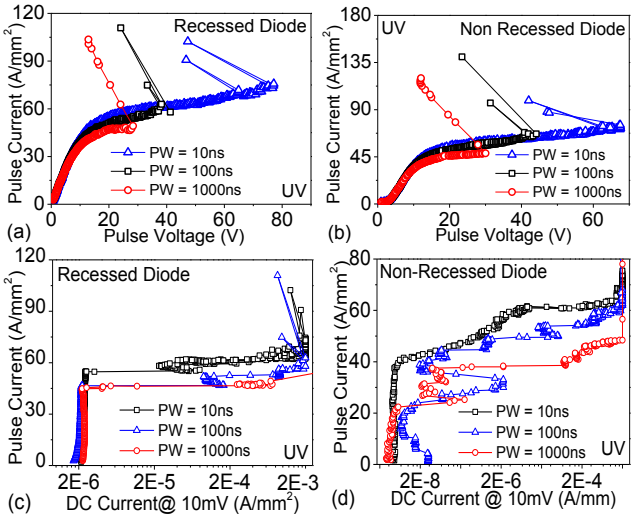

Figure 4: TLP characteristics of (a) recessed diode (b) non-recessed diode measured at different pulse width under UV condition. Degradation in spot measured DC current of (c) recessed diode and (d) non-recessed diode exhibiting softer degradation when compared to dark condition.

C. Effect of Anode Area

Figure 5 shows ESD robustness scales with anode perimeter rather than area, which is attributed to dominating side wall conduction in these diodes as illustrated in Fig. 1.

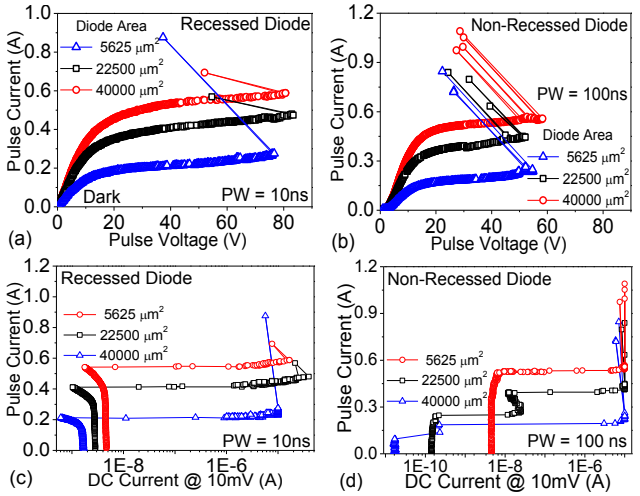

Figure 5: TLP characteristics of (a) recessed diode (b) non-recessed diode of different Anode area measured under dark condition. Figure shows (i) unchanged V_{SNAP} for different area device; (ii) I_{FAIL} scales with perimeter, not with area and (iii) current in nonlinear region increases and R_{ON} decreases with increase in diode area or perimeter. Degradation in spot measured DC current of (c) recessed diode and (d) non-recessed diode exhibiting hard early failure for large area devices.

D. Effect of Recess

Recessed diodes exhibited higher snapback/failure voltage than its non-recessed counterpart. Non-recessed diodes suffered hard degradation when stressed at different PWs under dark condition. However, recessed diode degrades gradually with increasing PW and anode area. This difference in degradation is attributed to different electric field distribution in the channel and in vicinity of Schottky contact as show in Fig. 6(a).

V. Analysis and Discussion

A. Power Law Behavior

Power-to-fail (P_{FAIL}), which is same as power-to-trigger device into snapback in case of GaN diodes ($P_{FAIL} = P_{TRIG} = I_{SNAP} \times V_{SNAP}$) is observed to fall with increasing PW; exhibiting power-law like behavior in all the cases as depicted in Fig 6b. This can be attributed to self-heating assisted enhanced thermionic injection across the Schottky barrier into the 2DEG channel. This further increases channel temperature via enhancement in optical phonon density and ultimately causes thermal runaway like failure. In addition to this longer stress times accelerates trap generation, which assist in early failure. The later aspect is described in subsequent sections.

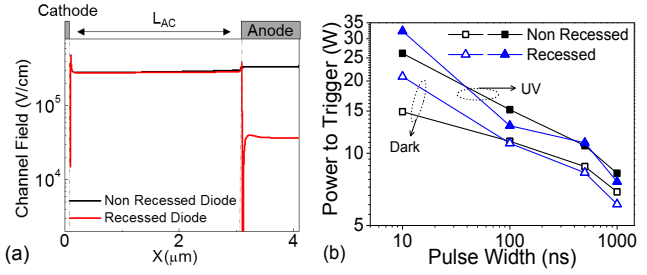

Figure 6: (a) Electric field profile along the channel for recessed and non-recessed diode. Non-recess diode has higher electric field in the channel. (b) Triggering behavior (power to trigger) of diode obeying power law like behavior under all stress configurations for recessed and non-recessed structures.

B. Interface Trap Generation and Correlation with High Current Failure

Fundamental nature and behavior of GaN/metal Schottky interface, under ESD conditions, is probed and reported for the first time in the present work. C-V measurement done in different regimes of TLP characteristics of recessed and non-recessed diode revealed following vital findings; (i) beyond a certain stress current, called safe operating stress current, interface trap density (D_{it}) increases by 4 orders of magnitude, as depicted in Fig. 7 – Fig. 9. (ii) Rise in D_{it} with stress, gets suppressed in case of longer stress pulses, which can be attributed to thermal annealing of the interface defects in presence of higher device self-heating [8]. (iii) UV exposure de-traps charges trapped at the interface and suppresses interface degradation.

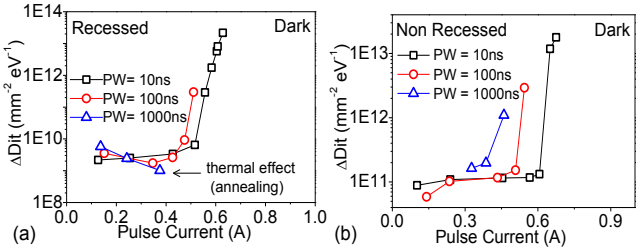

Figure 7: Change in interface trap density (ΔDit) in (a) recessed and (b) non-recessed diode with pulse current, during ESD stress of different PWs under dark condition.

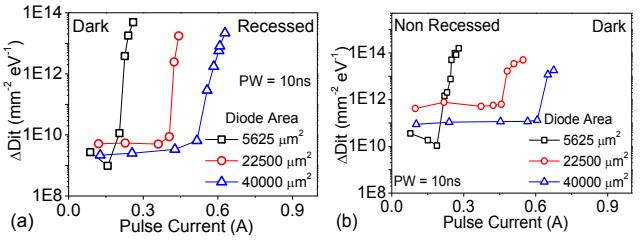

Figure 8: Change in interface trap density (ΔD_{it}) in (a) recessed diode and (b) non-recessed diode of different anode area, extracted as a function of stress current under dark condition.

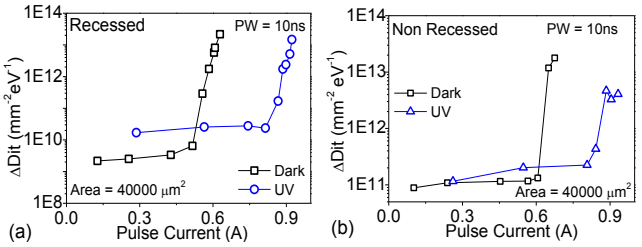

Figure 9: Change in interface trap density (ΔD_{it}) in (a) recessed diode and (b) non-recessed diode extracted as a function of stress current, compared under dark and UV conditions.

A unique correlation was discovered between device degradation and interface defect density (D_{it}) as shown in Fig. 10a. The leakage current and trap density were found to change together, i.e. increases at the same stress level. Moreover, it was found that the degradation was accumulative in nature, as depicted in Fig. 10b. On the fly DC I-V characteristics extracted in between TLP measurements shows gradual degradation of Schottky junction into an Ohmic one (Fig. 11a), which is due to lowering of Schottky barrier height (SBH) as shown in Fig. 11b. The lowering of SHB can be due to physical change at the interface or can be manifestation of increased trap density. This will be presented in the extended work.

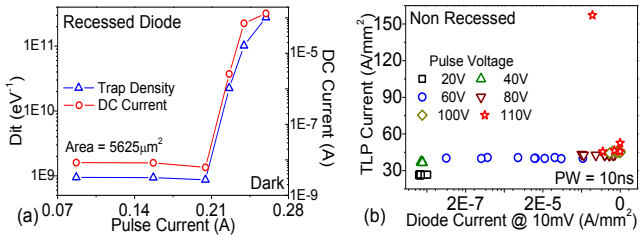

Figure 10: (a) Correlation between interface trap density (D_{it}) and spot measured DC current. (b) Diode leakage current measured after each pulse while stressing the device with 10 consecutive pulses.

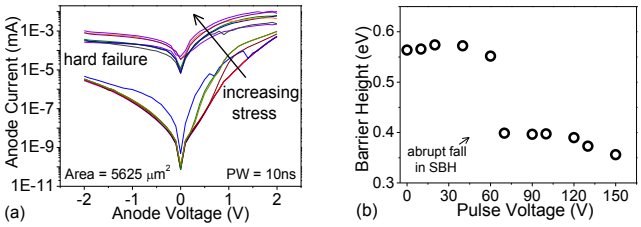

Figure 11: (a) DC I-V characteristics of non-recessed diode measured at regular intervals during a 10ns ESD stress applied at anode. (b) Change in Schottky Barrier Height with stress voltage.

VI. Failure Analysis

Post failure SEM micrographs of ESD damaged regions of diodes, as shown in Fig. 12, reveal presence of unique failure modes. For example, Fig. 12(a) shows metal migration from anode to cathode, when stressed using 1000 ns long pulse. EDX analysis revealed Au (14%) had migrated from Ni/Au anode contact. At very high pulse width, the lattice temperature in AlGaN/GaN diode is expected to be on the higher side, which can melt the contact metal(s). Also, high thermal stress accumulated in the strained AlGaN barrier and GaN cap layer, at high PW can peel off metal from contact pads as seen in Fig. 12(b). Failure at lower pulse width was found to be electrical in nature due to absence of self-heating. Field driven failures, example inverse piezoelectric induced cracks were observed, as depicted in Fig. 12(c). Pits and dislocations can also nucleate these cracks, as seen in Fig. 12(c) where crack originated from a pit/dislocation underneath the anode contact. No metal melt/migration is observed due to low self-heating at 10 ns pulse. Fig 12(d) shows device failure with a crack and metal melt at one of the diode corners in presence of high electric field at corners and high thermal energy available from 1000 ns PW.

VII. Conclusion

Recessed diode was found to offer better current conduction and higher failure current compared to non-recessed diode. The failure was discovered to be assisted by generation of traps at the Schottky – GaN interface of Schottky diode, which was found to increase with increasing ESD stress. The failure in

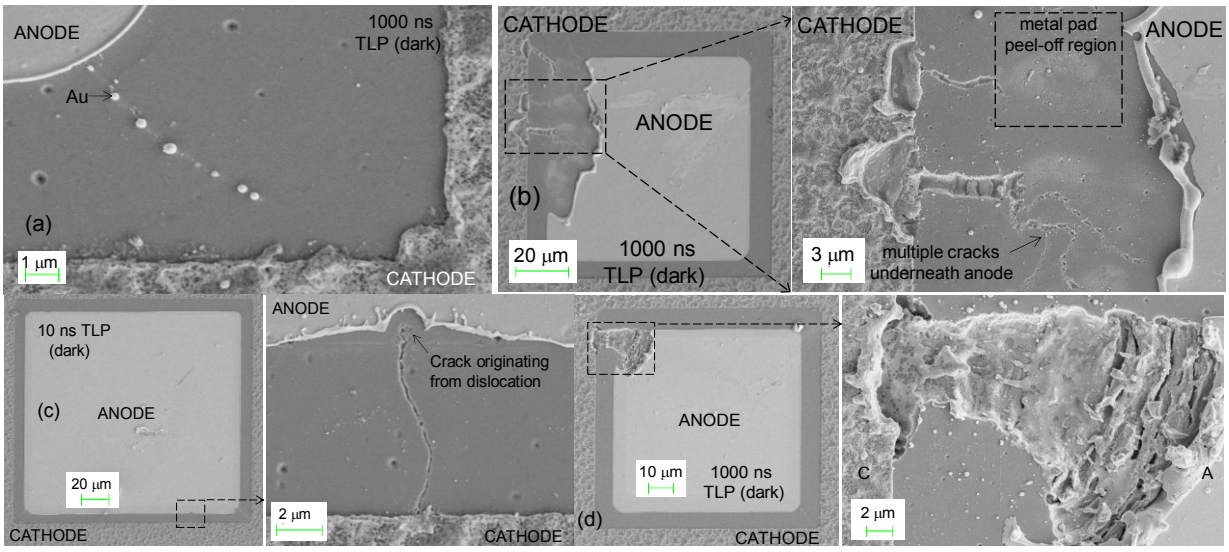

Figure 12: Post failure SEM micrograph of damaged regions in failed devices depicting different type of failure mechanisms. (a) Non-recessed Schottky diode failed at 1000 ns ESD stress at under dark condition due to metal migration from anode to cathode. EDX analysis revealed Au (14%) has migrated from Ni/Au anode contact. (b) Non-recessed diode failure occurred due to development of cracks under the anode pad and metal peel-off. Figure shows multiple fine cracks propagated and merged together to cause massive failure in region between anode-cathode contacts. (c) Recessed diode failed after 10 ns ESD stress. Anode-cathode region developed crack at high field due to inverse piezoelectric effect. Crack originated from a pit/dislocation underneath the anode contact. No metal melt/ migration are observed due to missing self-heating at 10ns pulse. (d) Recessed diode failed with massive crack and metal melt at one of the diode corners in presence of high electric field at corners and high thermal energy available from 1000 ns ESD stress.

these diodes was cumulative in nature and followed a power law like behavior. In case of recessed diode trap generation and failure was found to be abrupt, which was gradual in case of non-recessed diode. The stress induced trap generation was found to slow down when UV light was exposed, which was due to fast de-trapping of carrier. Finally, unique failure modes were identified.

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