Trap Assisted Avalanche Instability and Safe Operating Area Concerns in AlGaN/GaN HEMTs

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***Abstract*— This work reports the very first systematic study on the physics of avalanche instability and SOA concerns in AlGaN/GaN HEMT using sub-µs pulse characterization, post stress degradation analysis, well calibrated TCAD simulations and failure analysis by SEM and TEM. Impact of electrical, as well as thermal effects on SOA boundary and avalanche instability are investigated. Trap assisted cumulative nature of degradation is studied in detail, which was discovered to be the root cause for avalanche instability in AlGaN/GaN HEMTs. Post failure SEM/TEM analysis reveal distinct failure modes in presence and absence of carrier trapping.**

***Index Terms*—Avalanche Instability, Trapping, Safe Operating Area, Failure Modes, Gallium Nitride (GaN), High Electron Mobility Transistor (HEMT).**

I. Introduction

Gallium Nitride on Si based High Electron Mobility Transistor (HEMT) has invoked great interest for high power and high frequency applications. The attractive properties of GaN, like wide bandgap (3.4 eV), high breakdown field (3.3 MV/cm) and low dielectric constant (9) boast GaN as potential replacement of Si for power device technology. Moreover, high 2DEG density (10^{13} cm^{-2}), high electron peak velocity (2.5×10^7 cm/s) and high electron saturation velocity (1.5×10^7 cm/s) offered by AlGaN/GaN hetero-junction over Si substrate, promises outstanding device performance at the cost much lower than its SiC and Diamond based counterparts. However, reliability of AlGaN/GaN HEMT on Si, has increasingly become a challenge to its widespread adoption. Long term reliability of these devices has been greatly studied in literature [1]-[4]. However, ability of GaN HEMT to handle high power under extreme conditions and related safe operating area (SOA) concerns are largely missing in literature [5], including the failure mechanisms which determine the SOA boundary. SOA and avalanche instability are still considered to be a serious research subject for Si or SiC power MOSFETs [6], the AlGaN/GaN HEMT is certainly not an outlier. Keeping in mind the gap, this work is the very first systematic study on the physics of avalanche instability and SOA concerns in AlGaN/GaN HEMT using sub-µs pulse characterization, post stress degradation analysis, well calibrated TCAD simulations and failure analysis by SEM and TEM.

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II. Device Fabrication and Test Set-up

Normally-On HEMTs were fabricated on a AlGaN/GaN layer stack (Fig.1), which was grown on 2-inch Si (111) using MOCVD. Devices of 3 µm gate length and 100 µm width were processed with different source–to-drain spacing (L_{SD}), using UV lithography. MESA isolation among devices, was achieved using Chlorine based ICP-RIE. S/D contacts were realized by using Ti/Al/Ni/Au metal stack, deposited using E-beam evaporation and post deposition anneal to form ohmic contact with 2DEG. Finally, Ni/Au Schottky gate was deposited and annealed. Devices were processed with (Al_2O_3) and without surface passivation. Pulse I-V characterization of AlGaN/GaN HEMT devices was performed to determine the SOA boundary and failure threshold. To study the failure mechanism, linear drain-to-source dc current of the device was measured after each stress pulse. To study effect of bulk and/or surface traps, measurements were performed in presence and absence of UV (365 nm) light.

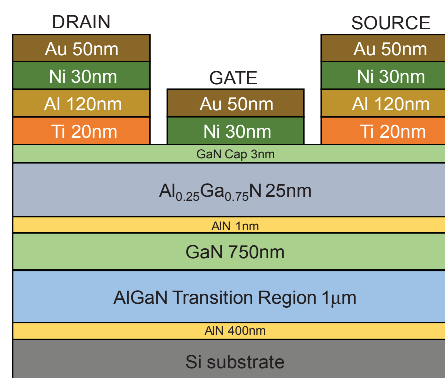

Fig. 1: Cross-sectional view of AlGaN/GaN layer stack and HEMT under test. HEMT devices are stressed in dark and UV (365 nm) light condition using pulse setup with varying pulse widths.

III. SOA Boundary and Carrier Trapping

Pulse I-V characteristics extracted for HEMTs with passivation, under dark and UV light condition, depict an improvement in SOA boundary with UV exposure (Fig. 2a-b). Similar observations can be made from Fig. 2c for devices without passivation, which shows that SOA boundary improves for shorter pulse widths and in presence of UV exposure. Improved SOA boundary for shorter stress times

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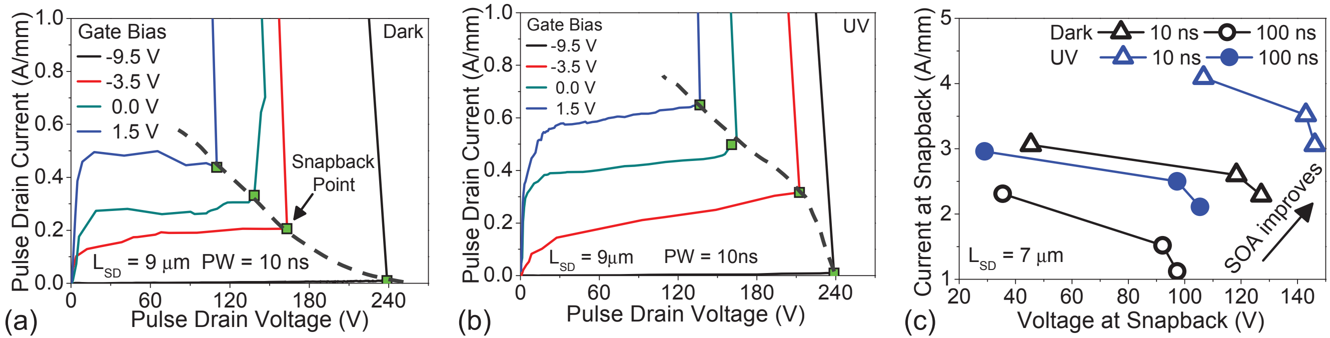

Fig.2: Pulse I-V characteristics of HEMT with surface passivation extracted (a) under dark condition and (b) with UV exposure. Carrier trapping in different regions degrade device causing early failure. UV exposure improves SOA by assisting in carrier de-trapping and suppresses degradation, which avoid premature device failure. Snapback point shown here marks the onset of device failure and SOA boundary. (c) SOA boundary of HEMT devices (without surface passivation) stressed using different pulse widths under dark and UV condition.

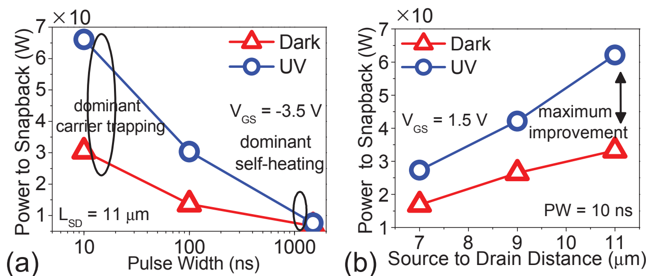

Fig. 3: (a) Power to snapback as a function of pulse width extracted under dark and UV condition. While exhibiting power law behavior presence of UV improves power to snapback at shorter pulses. (b) Power to snapback as a function of source – drain spacing. It increases linearly with L_{SD} and shifts upwards with UV exposure.

indicates presence of thermal effects, whereas the same in case of UV exposure signifies role of surface and/or buffer traps. On the verge of failure i.e. at snapback point, the power-to-snapback was observed to decrease with increase in pulse width, exhibiting a power law like behavior, under both dark and UV light conditions (Fig. 3a). Power-to-snapback for longer stress times remains same for both UV and dark condition; but differs by 2× at 10 ns. Furthermore, linear scaling of power-to-snapback with source-to-drain spacing (L_{SD}) is also observed (Fig. 3b). After each stress pulse linear drain-to-source dc current is extracted, and is shown in Fig. 4. Figure 4(a) shows that when devices were stressed under dark condition, the device degraded in a cumulative fashion above a certain critical current. Device degradation, after stress, is known to be due to carrier trapping [2]. This is further validated by experiments under UV exposure. Figure 4(b) shows that device degradation is absent in presence of UV exposure. The trends discussed above can be explained as follows: at higher drain field channel electrons gain sufficient energy to surmount 2D quantum well and get trapped in the surface traps and/or buffer traps, which degrades the device performance under dark condition. UV exposure assists in carrier de-trapping and suppresses the trap originated device degradation. Furthermore, it was found that device degradation linearly increases with PW, due to longer time and higher temperature/ thermal energy_available for carrier trapping and it linearly decreases with source to drain distance, i.e. channel field (Fig. 4c). Figure 5a further depicts cumulative nature of device degradation under dark condition, which was missing under UV exposure. Moreover, Fig. 5b reveals that carrier trapping takes at the gate edge and in the drift region, which degrades the Schottky barrier, shifts the threshold voltage and increases the gate leakage and UV exposure de-traps the carriers and minimizes Schottky degradation as clear from Fig. 5c. Given that SOA boundary

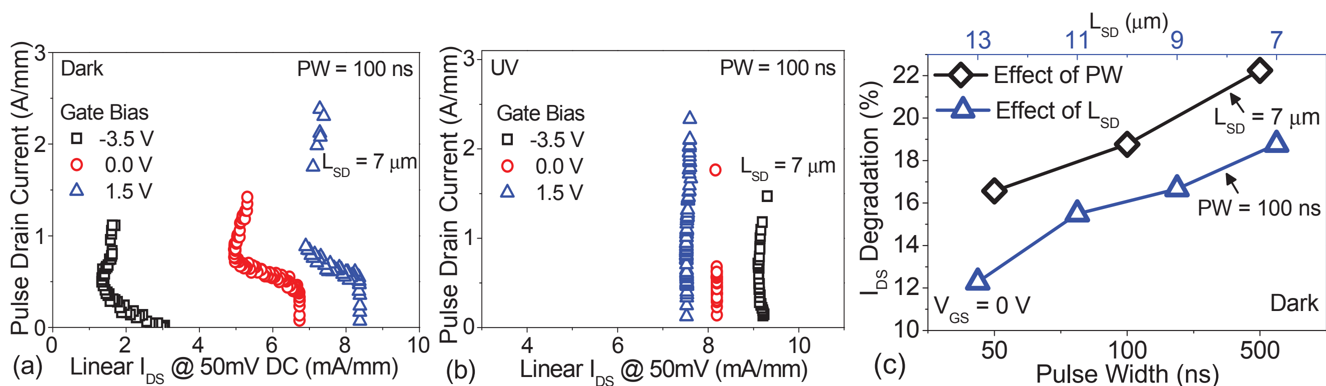

Fig. 4: Linear drain-to-source current measured after each pulse stress across the device under (a) dark and (b) UV condition. Unique current degradation trend can be observed after each voltage pulse, under dark condition, which is absent under UV light condition. Negligible degradation in presence of UV light is attributed to carrier de-trapping. (c) Degradation in linear drain current measured at 50 mV DC, under dark condition as a function of pulse width and source to drain spacing.

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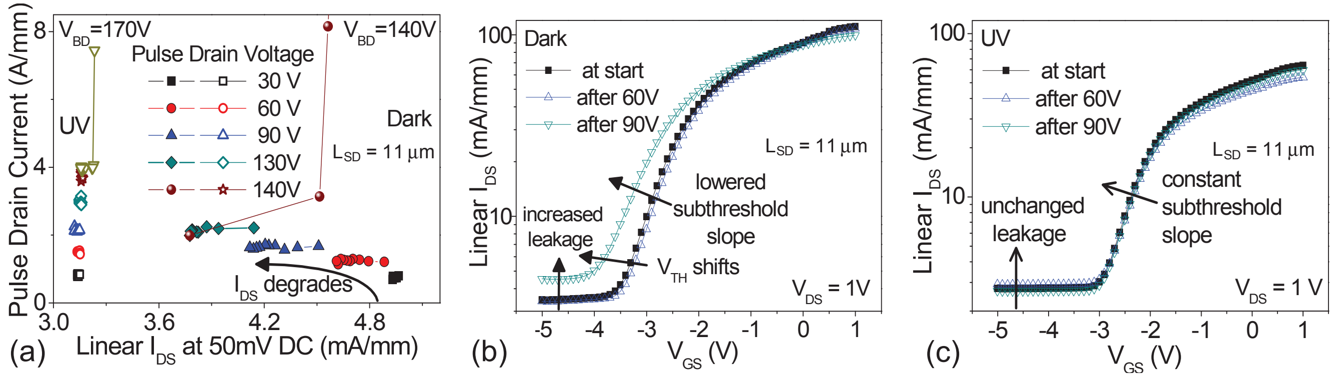

Fig. 5(a) Cumulative degradation extracted by applying set of ten constant voltage pulses before increasing its amplitude. A cumulative degradation is visible under dark condition, which is missing in presence of UV light. (b) DC transfer characteristics measured after stressing device using a set of ten pulses under Dark and (c) UV conditions. In dark condition, device's off-state leakage has increases, threshold voltage and subthreshold slope are affected too, which is absent in presence of UV exposure.

improves, when device degradation was absent, it can be concluded that carrier trapping assists in avalanche instability and early snapback (explained below). At longer stress pulses, independent of device degradation, which was present in both the cases, device fails due to electro-thermal instability.

IV. Trap Assisted Avalanche Instability and SOA Failure

TCAD simulations (Fig. 6) depict shift in surface as well as channel field when buffer traps were increased. Similarly, it reveals that increasing the surface trap density increases the field at the gate edge, both inside the channel, as well as at the surface. Beside the shift in lateral field, for higher buffer trap concentration, field strength also increases under the drain contact. This leads to localized electron – hole pair generation. The excess holes, which are collected at source, form a parasitic path below the GaN buffer (Fig. 7). Due to finite defect density of MOCVD grown GaN/AlGaN, the trap generation and carrier trapping occurs non-uniformly across the device width. This leads to formation of localized regions, where carrier trapping is higher compared to rest of the device's active region. These regions in turn see an early shift in electric field peak towards drain, which forms localized parasitic path(s). These localized parasitic paths lead to formation of current filament, which is evident as avalanche instability or snapback in the I-V characteristics shown in Fig.8. Beside failure analysis results (presented below), the avalanche instability due to filament formation can be validated from pulse to pulse instability observed in Fig. 8a, when measured under dark condition. In this case, device forms a filament however, it survives thermal failure due to short duration of applied stress. As a result, device tries to enter into snapback state multiple times, before experiencing a localized thermal fail at higher currents. However, the same instability was absent under UV exposure as shown in Fig. 8b.

V. Failure Analysis

Under dark condition, failure was found to occur in the G/S region (Fig.9a-b), while under UV exposure device was found to fail in G/D region (Fig. 9c). Figure 9a and 9b clearly show multiple failure spots in the G/S region, which is attributed to hole accumulation under gate and formation of localized parasitic/filament paths. This corroborates with the filament and avalanche instability theory presented above. In addition to this, a significant Ga out diffusion under the gate can also be found from TEM pictures (Fig. 9b). As presented above, in absence of traps, i.e. in presence of UV light, the peak electric field lies at gate edge towards drain. This leads to formation of hotspot at the drain side of gate edge (Fig. 7b), generating thermal stress in the vicinity of gate which results in cracking (Fig. 9c). Under the influence of G-D electric field, the crack propagates towards the drain. Hot spot at the gate also peels-off the gate metal (Fig. 9c), which can migrate from gate-to-drain, along the low energy path provided by crack, under the influence of gate-to-drain field.

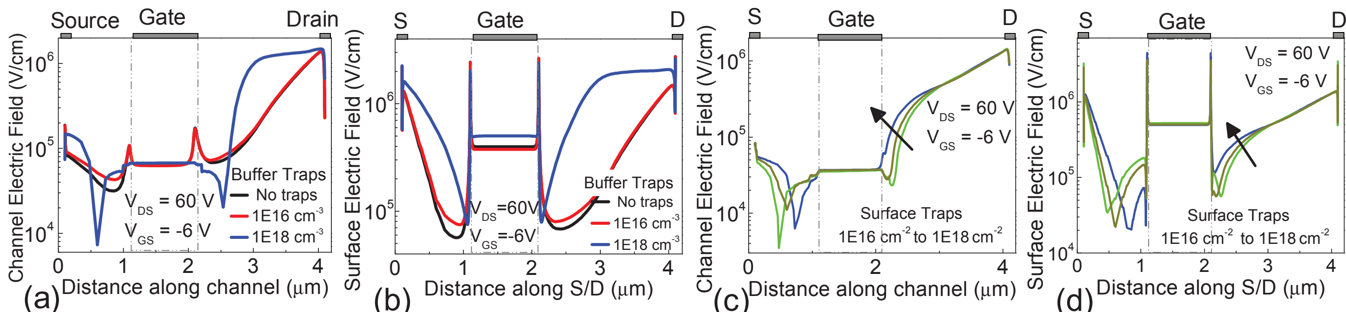

Fig.6: (a), (c) Channel and (b), (d) surface electric field extracted using TCAD simulations while varying (a), (b) GaN buffer traps and (c), (d) surface traps. When buffer trap conc. was increased the surface and channel fields in gate-drain region increases and peak field shifts from gate edge towards drain. While considering only surface traps, field at the gate edge increases when surface trap concentration was increased.

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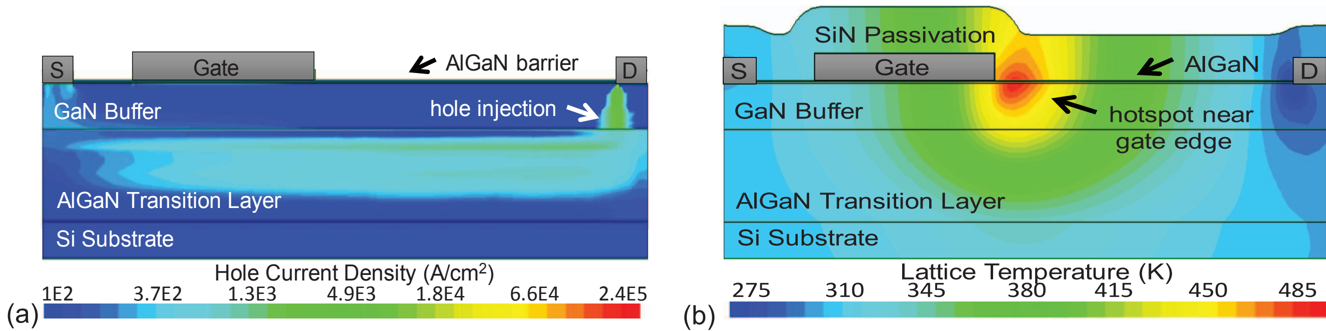

Fig.7 (a) TCAD contour depicting hole distribution at the device breakdown, under -6V gate bias condition. Excess holes generated at near drain edge due to impact ionization are injected into the buffer, which are collected at the source, forming parasitic S/D short path in buffer. (b) Temperature distribution across the device depicting hotspot near drain side of gate edge.

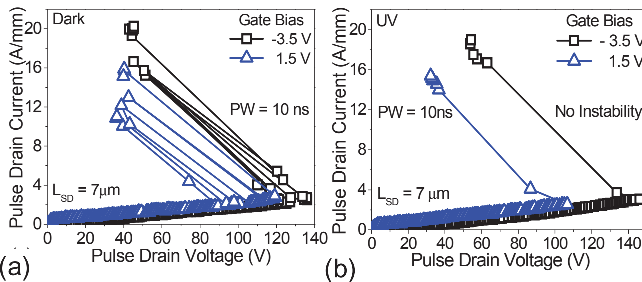

Fig. 8: (a) Snapback instability observed in I-V characteristics extracted dark conditions using 10ns PW. This is attributed to electrical instability caused by carrier trapping in different device regions. (b) Absent snapback instability in presence of UV exposure.

VI. Conclusion

For the first time physics of avalanche instability and SOA boundary in AlGaN/GaN HEMT are studied systematically. It was found that trap generation and carrier trapping leads to electric field shift and peaking towards drain edge. In case of non-uniform carrier trapping across the device width, drain field peaks in localized regions along the device with. This causes localized generation of excess holes, which in-turn forms localized parasitic path under the buffer, from source to drain. This results in formation of filaments, which triggers early instability and lowers the SOA boundary. Such a trap assisted avalanche instability was found to be absent when

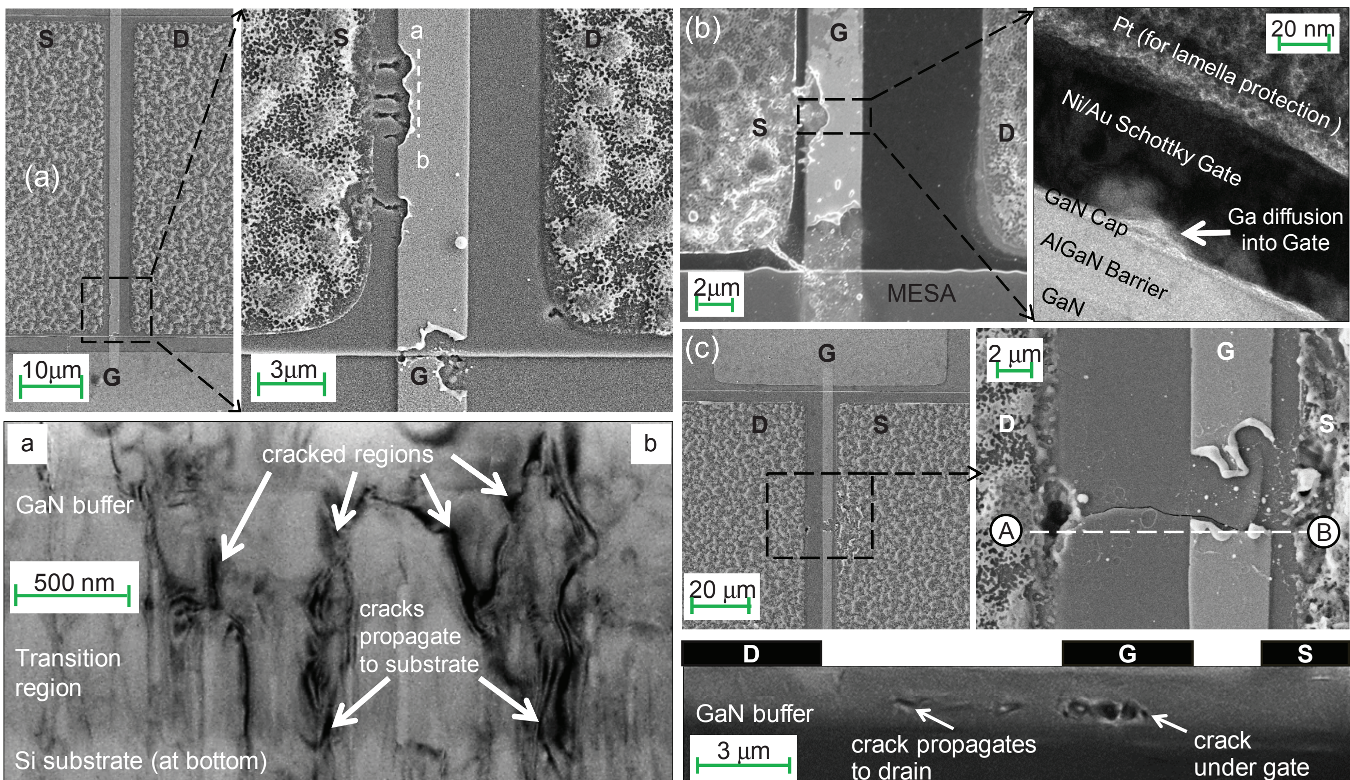

Fig.9: Post failure SEM and TEM images depicting different types of failures and failure mechanisms dominant during test under dark and UV conditions. (a) HEMT failed under dark condition, stressed using 10ns pulses, shows multiple damage sites in S-G region. Cross-sectional TEM along line 'a-b' depicts cracks running down to buffer region/transition region. (b) HEMT failed under dark condition, stressed using 10ns pulses, shows damage in S-G region and failure at MESA Schottky junction. TEM analysis of damaged region reveals Ga out-diffusion into Ni/Au Schottky gate. (c) HEMT failed under UV condition, stressed using 10ns pulses, shows damage in G-D region. Cross-sectional SEM image taken along line 'A-B' depicts cracks underneath the drain side of gate edge which propagated towards the source.

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carrier trapping was suppressed using UV light exposure while stressing the devices. TCAD and failure analysis results nicely corroborate with the physics of avalanche instability presented.

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