ESD Behavior of Large Area CVD Graphene RF Transistors: Physical Insights and Technology Implications

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Abstract—**In this work, for the first time, we have used a matured graphene technology platform for ESD physics explorations while investigating implications of various design and technology options. Impact of diffusive vs. ballistic carrier transport and top-gate vs. back-gate on failure mechanism is investigated. A unique contact limited failure in graphene transistors is reported. Physical insights on current saturation in graphene FET and unique step by step failure in dielectric capped transistors is presented for the first time. Moreover, device degradation under ESD time scales and its implications on current saturation are revealed. Finally, influence of various top-gate designs on the ESD performance is reported. The new physical insight and matured graphene FET technology has enabled record high failure current.**

Index Terms— **Graphene, Electrostatic Discharge, Chemical Vapor Deposition (CVD),**

I. Introduction

It's been over a decade since Graphene is being explored as a channel material for THz applications [1]–[3], which is attributed to its extraordinary electrical and thermal properties [4]-[5]. However, it was very recent when long term and ESD reliability of graphene FETs received attention [6]-[8] which without exaggeration is at a nascent stage. This is attributed to (i) unavailability of high quality large area graphene in initial years, (ii) lack of matured technology and (iii) use of back-gated geometries for explorations. For instance, ESD behavior of graphene was first reported [7] using the exfoliated material and more recently [8] using CVD graphene, both without a top-gate or dielectric passivation. In this work, for the first time, we have used a matured graphene technology platform with record performance [9] for ESD physics explorations while investigating implications of various design and technology options.

II. Graphene Device Fabrication & Designs under Test

High quality CVD grown Graphene on Cu (Fig. 1a) was transferred to Si/SiO_2 substrate using PMMA based wet transfer technique, which was then patterned using electron beam lithography and O_2 plasma. After contact engineering, source/drain (Pd) pads were deposited using UHV electron beam evaporation, followed by lift-off and high-temperature anneal. After a blanket atomic layer Al_2O_3 deposition and post-deposition anneal gate metal was deposited, followed by a post-metallization anneal. At last Al_2O_3 over S/D contact pads was removed using RIE. The developed technology has resulted in record high performance [9]. For ESD investigations following designs were fabricated with electrical width up to 40 mm: (i) back-gated graphene FET without top-dielectric capping, (ii) back-gated graphene FET with top-dielectric capping, and (iii) top-gated RF graphene FET with gate-to-S/D overlap or under-lap (Fig. 1). ESD events were emulated through a commercial TLP tester.

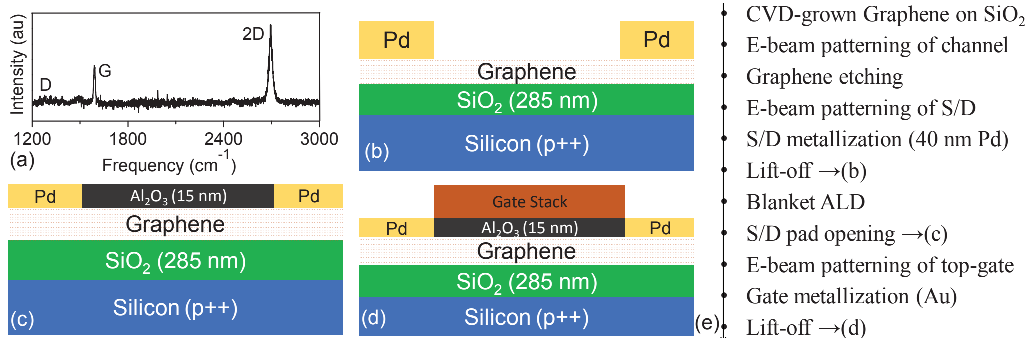

Fig. 1: (a) Sharp 2D peak and suppressed D peak in Raman spectra of post-transfer graphene indicates pristine nature of monolayer graphene. (b)-(d) Schematic of various graphene FETs (GFETs) architectures investigated. (b) back-gated FET (c) back-gated FET with dielectric capping and (d) top-gated FET with high-k metal gate stack (e) process flow.

III. Carrier Transport and Related Failure under ESD Condition

The electro-thermal transport during ESD event is investigated using back-gated graphene FET design without

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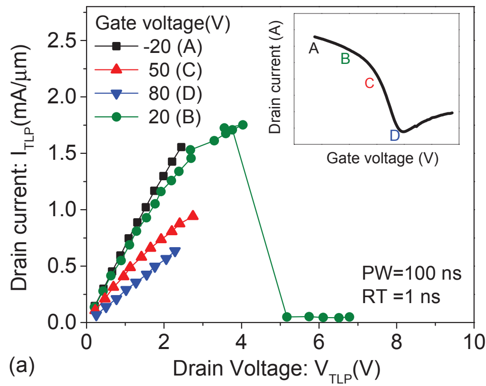


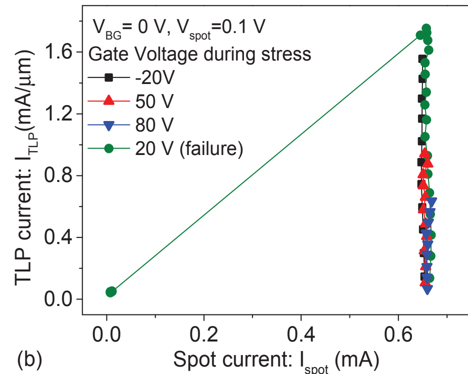


Fig. 2: (a) TLP IV characteristics of back-gated GFET in ambient condition at different gate voltages. Device was stressed till failure only for back-gate voltage (V_{BG}) = 20 V. Inset shows the DC I-V characteristics of device under stress. (b) DC spot current measured after each pulse. Abrupt collapse in TLP current or DC spot current is the signature of failure. **Note:** In case of abrupt failure, post failure data points are not shown in other figures for clarity.

dielectric capping, which is extended later to technologically relevant architectures. Figure. 2 shows typical TLP I-V characteristics of graphene FET at different gate bias, depicting abrupt failure when stressed under ESD conditions. Clearly matured graphene FET technology and high quality CVD graphene has resulted in record high failure current of 1.75 mA/µm (Fig. 3). Figure. 4 reveals an early saturation in drain current with increasing channel length, which is attributed to shift from quasi-ballistic transport in short channel FETs to diffusive transport in long-channel devices. Compared to diffusive channel, carriers in quasi-ballistic channel encounter relatively less scattering centers, which leads to electron - phonon scattering only at the drain contact. Contrary to quasi-ballistic transport, in diffusive channel, carriers experience an increased scattering in the channel region than in the contacts, which in turn reduces the carrier mobility and results in early saturation in drain current. Fig. 4 further depicts that early saturation in drain current lowers the failure current. Figure. 5 shows that devices with quasi-ballistic channel fails due to thermal-assisted breakdown of contacts, while excessive heating of the channel results in failure of diffusive channel FETs. Consequently, failure current due to channel limited breakdown increases linearly with device width, while the same due to contact limited

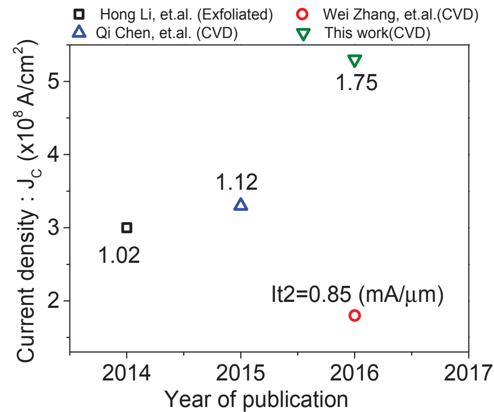
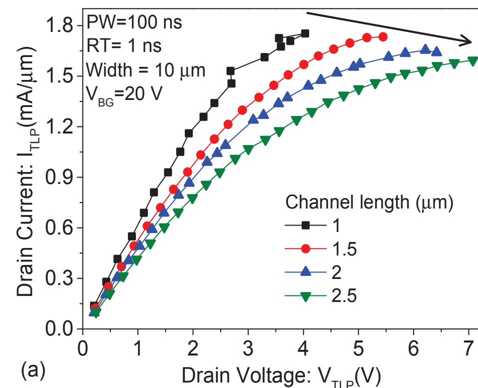


Fig. 3: Summary of failure current density, under ESD condition, reported till date. Failure current (mA/µm) per monolayer is listed too next to the respective symbols.



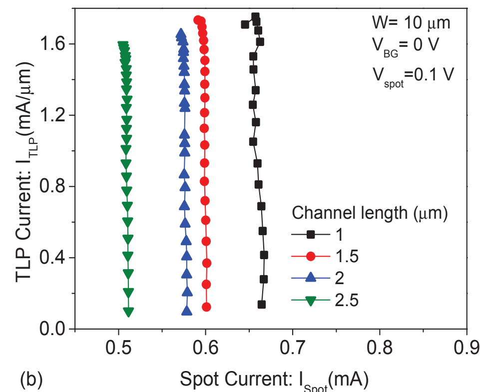


Fig. 4: TLP IV characteristics of back-gated GFET without dielectric capping for different channel lengths. With increase in channel length nature of carrier transport shifts from quasi ballistic to diffusive, consequent of which reduction and saturation in current is observed. (b) Spot measurements does not show any change, corroborating the fact that length-dependent change in TLP I-V is indeed a transport behavior and not pre-failure degradation.

breakdown saturates with increase in FETs electrical width. It is worth highlighting that here graphene is an atomically thin layer, whereas S/D metal pads are 100 nm thick. Figure. 5 further reveals importance of S/D contact design for ESD robust graphene transistors.

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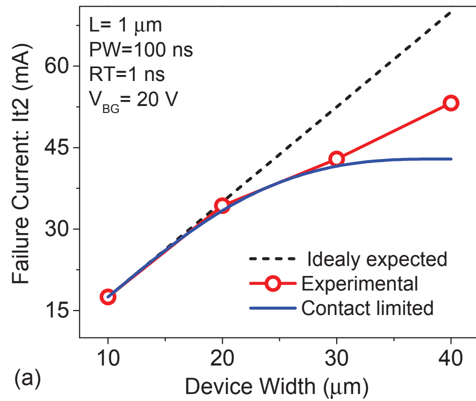


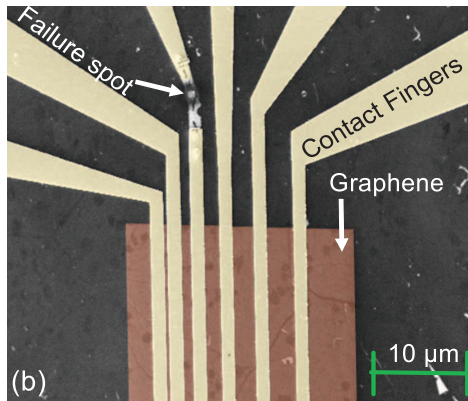
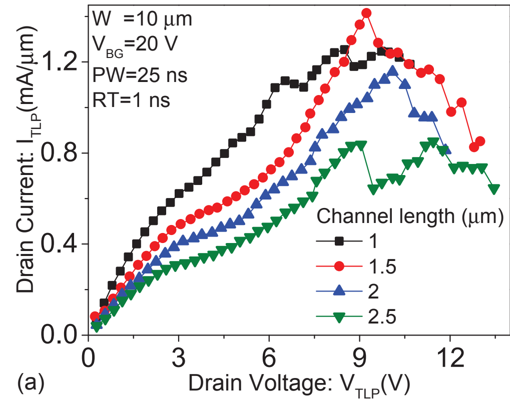


Fig. 5: Failure current as a function of device width (W). Ideal trend shows channel limited failure, where It2 scales linearly with W. In case of contact limited failure current saturates with W. Obtained trends revel electro-migration of contact for larger device widths. It was found that failure was located in graphene channel for W ≤ 20 µm, while the failure location shifts to contact fingers for width >20 µm. To validate our argument, devices with W=40 µm was fabricated with wider metal, which resulted in higher It2 compared to expected saturated It2 (blue curve). (b) False color SEM image showing the S/D contact failure due to electro-migration.



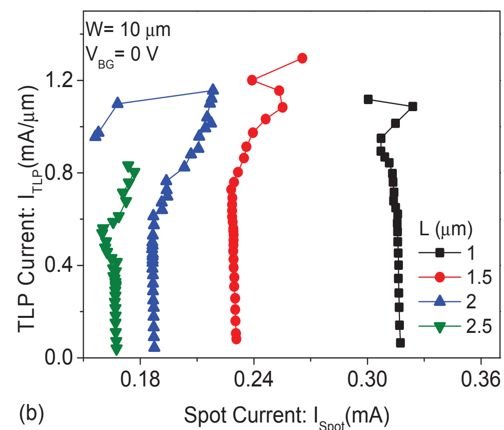


Fig. 6: TLP characteristics of back-gated devices stressed using 25 ns TLP pulse reveals role of gate dielectric traps in shifting the Dirac point and delaying the onset of saturation. (b) Increase in spot current measured after each pulse confirms shift in the Dirac point before device failure.

Figure. 6 depicts that when graphene devices were stressed using shorter TLP pulses the device survived till higher voltages, however higher, fields lead to carrier trapping in SiO_2, which can be seen in form of current fluctuations and instabilities. It can also be noted that the trapped carriers shift the Dirac point, which in turn increases the drain current beyond the onset of current saturation. The shift in the Dirac point of the graphene channel is evident from the spot current data in Figure .6(b). At higher stress levels, the DC spot current increases before it finally collapses due to the failure. This behavior is attributed to the carrier trapping in SiO_2. Finally, it was found that unlike conventional silicon-based devices, which exhibit a power law like behavior, graphene device shows a very week power-to-failure dependence on stress time (Fig. 7).

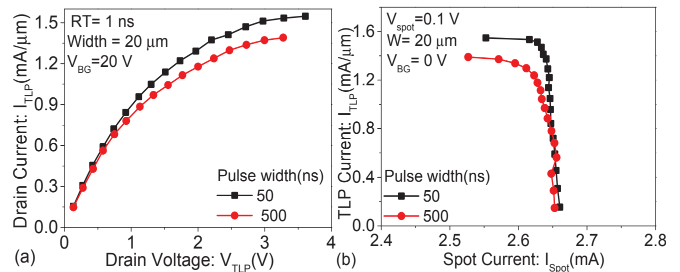


Fig. 7: TLP I-V characteristics of GFET stressed using shorter and longer pulses depicting insensitivity of failure current towards stress time.

IV. High-κ Dielectric Capping and its Implications on ESD

This section extends investigation to technologically relevant high-k dielectric-caped graphene FET device. Conventionally, under excessive heating, graphene channel fails due to oxidation of carbon atoms. However, Figure. 8 reveals that despites the low oxygen content in passivated

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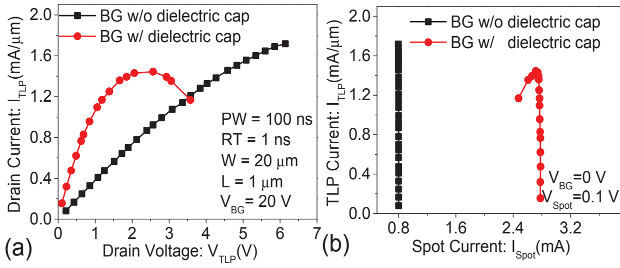

Fig. 8: (a) TLP IV characteristics of back-gated GFET, with and without dielectric cap. Early current saturation and failure in capped devices is due to higher self-heating. (b) Reduction in spot current with increasing I_{TLP} is a signature of gradual failure of capped graphene FET.

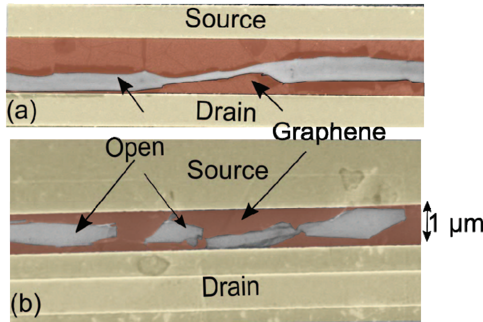

Fig. 9: False color SEM Image of (a) GFET without dielectric cap. (b) with dielectric cap. Failure in capped devices is in patches contrary to a continuous failure spot in w/o dielectric cap devices, confirming the gradual failure mechanism with dielectric on top.

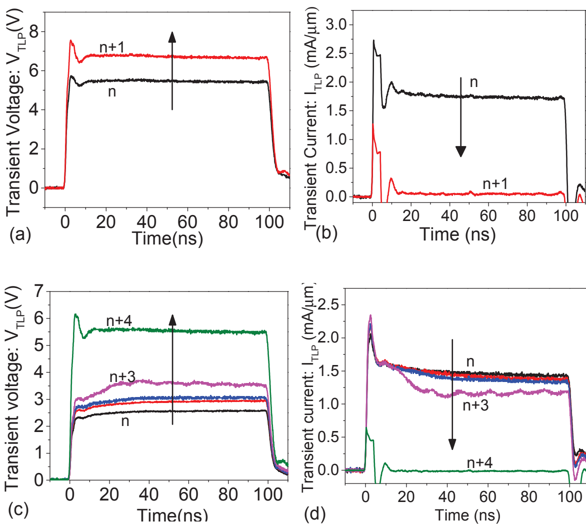

Fig. 10: Transient analysis of back-gated GFET (a) & (b) without dielectric cap, (c) & (d) with dielectric cap at the onset of failure. Direction of arrow indicates (a/c) increase in pulse voltage amplitude and (b/d) subsequent collapse in drain current with increasing ESD stress amplitude in steps. Drain current collapses abruptly at the onset of failure in devices without cap, whereas capped device shows gradual collapse in drain current.

devices, the power-to-failure is lower compared to devices without passivation. It was found (Fig. 9) that unlike devices without passivation where quasi-ballistic transport is observed, the dielectric capping introduces boundary

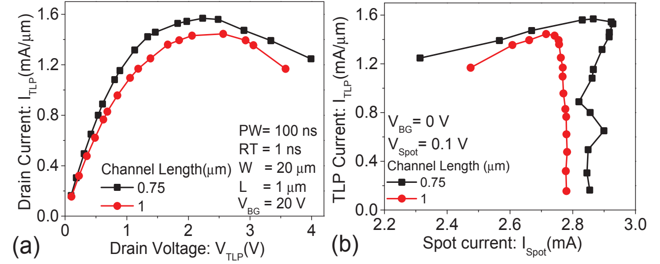

Fig. 11: TLP I-V characteristics of dielectric capped GFET for different channel lengths. Increased onset of current saturation for shorter channel length is evident.

scattering in the channel. This spreads heat across the whole channel and leads to diffusive transport (Fig. 9). Moreover, contrary to abrupt/hard failure of graphene FETs in ambient, a gradual failure is observed in case of dielectric-capped graphene FETs. This is attributed to reduced degree of freedom for the carbon to get oxidized, which makes the failure gradual (step-by-step), as depicted in Figure. 9 - 11. Figure. 12 pictorially summarizes ways in which different graphene devices fail under ESD condition.

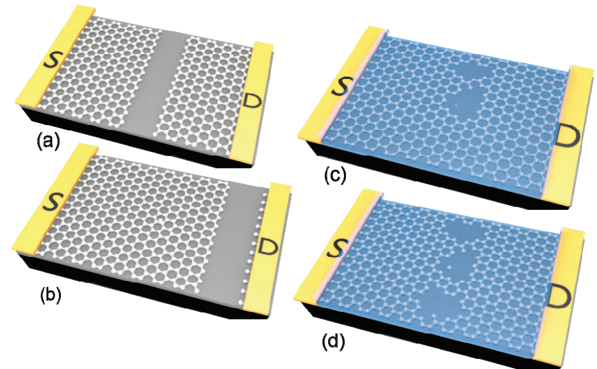

Fig. 12: Atomistic view of device failure: (a) Back-gated GFET w/o dielectric cap with diffusive channel, (b) Back-gated GFET w/o dielectric cap with ballistic transport. In these two cases, continuous failure spot is depicted. (c) Back-gated GFET w/ dielectric cap showing failure patches after first failure and (d) back-gated GFET w/ dielectric cap showing failure patches after eventual failure. Cyan color depicts ALD Al_2O_3.

V. High-κ Metal Gate Graphene FET

Figure. 13 reveals that the top-gated graphene transistors fail at a higher current and power compared to their back-gated (w/ cap) counterparts. The improved ESD robustness can be attributed to efficient heat removal from the graphene channel through the metal gate. Presence of hot spot at the drain edge and heat removal by gate metal is confirmed by gate-to-S/D under-lap design, which depicts lower ESD robustness compared to over-lap design. Consequently, position of top-gate electrode plays a crucial role in removing heat energy from the channel. The top-gate not only affects the failure mechanism, but was also found to dynamically shift the Dirac point. This is attributed to trapping of charge carriers in gate

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dielectric, which is prominent on top-gates devices compared to back-gated devices. Finally, Figure. 14 depicts impact of vertical gate field on the failure threshold s. The difference in the ON resistance is attributed to the difference in the operating point w.r.t top-gate. Under floating gate condition, the gate to drain capacitance dynamically charges the top-gate, which leads to early carrier velocity saturation and failure.

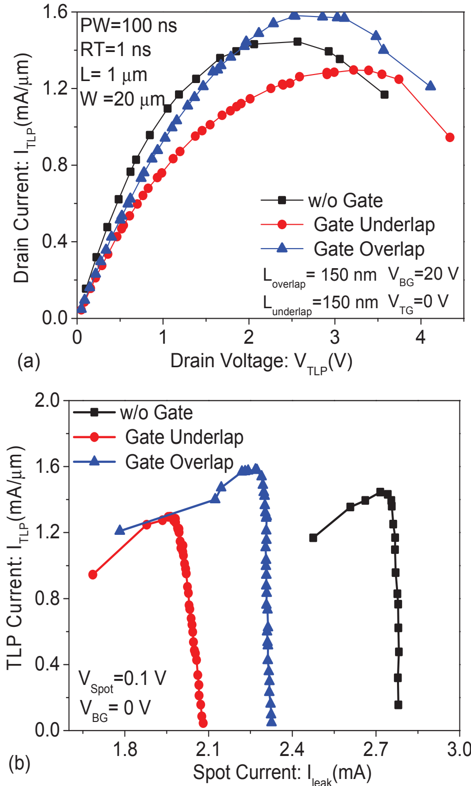

Fig. 13: (a) TLP I-V characteristics of GFET compared for devices with underlap top-gate, with overlap top-gate and without top-gate. In all cases the top-gate is grounded. Placing a high-k metal gate stack over the channel improves the failure current attributed to efficient cooling of graphene channel through gate metal. (b) Dynamic shift in Dirac point of devices studied after each stress pulse.

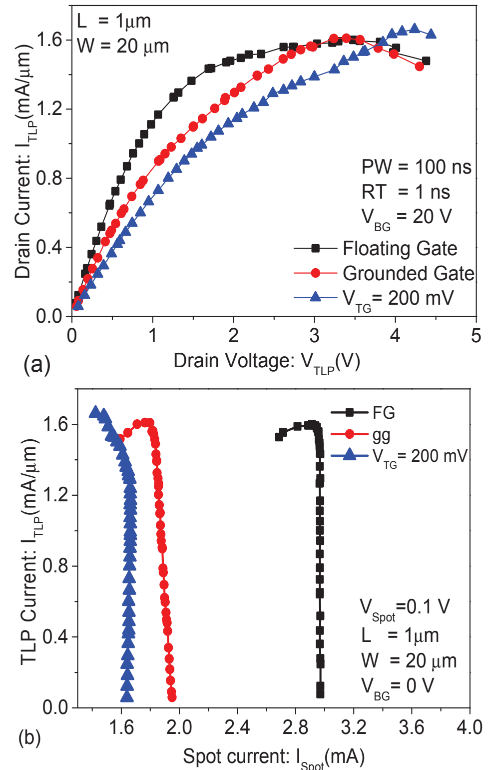

Fig. 14: TLP I-V characteristics of top-gated GFET under different biasing schemes. Top-gate device, biased at 200 mV, shows highest failure current and shift in Dirac point beyond the onset of current saturation, which is attributed to generation of traps in top-gate dielectric. (b) Change in spot current with increasing TLP current confirms shift in Dirac point due to carrier trapping in top-gate dielectric.

VI. Conclusion

Saturation in drain current, just before failure, with increasing channel length was observed, which was found to be due to shift from quasi-ballistic transport in short channel FETs to diffusive transport in long channel devices. However, it was found that failure current is more or less insensitive to channel length. Furthermore, it was found that devices with quasi-ballistic channel fails due to thermal-assisted

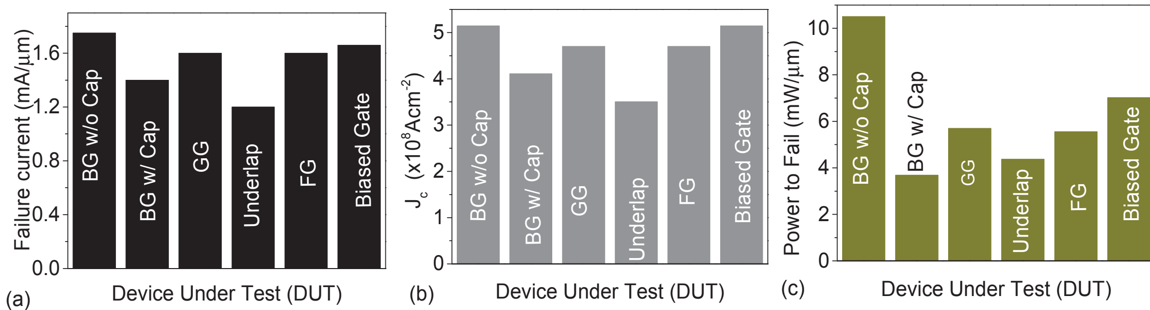

Fig.15. Comparison of (a) failure current, (b) maximum current density and (c) power-to-fail for various device architectures and biasing schemes investigated in this work. Here BG w/ cap and BG w/o cap are back-gate GFET with and without dielectric cap respectively. GG is the grounded top-gate architecture, under-lap is the gate under-lapped and grounded, FG is the GFET with floating top-gate and biased gate is the top-gate device biased at 200 mV.

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breakdown of drain contact or graphene channel next to drain contact, while diffusive channel FETs experience excessive heating of the graphene channel and oxidation. It was observed that the devices stressed using shorter pulses (<25 ns) survive higher voltages, however leads to device degradation due to carrier trapping in SiO_2. Moreover, an absence of power law like behavior was discovered. In other words, failure current was found to be insensitive to stress time. This work reveals that devices without dielectric capping fail abruptly, whereas devices with dielectric capping or top-gate stack fails gradually. Interestingly, power to fail was found to be lower for devices with dielectric capping. Finally, top-gated devices were found to have better ESD robustness when compared to devices with dielectric capping, which is due to efficient heat removal from the graphene channel through the metal gate. The detailed physical insight and matured graphene FET technology has enabled record high failure current (Fig. 15).

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