Novel Surface Passivation Scheme by Using p-Type AlTiO to Mitigate Dynamic ON Resistance Behavior in AlGaN/GaN HEMTs—Part II

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***Abstract*— The underlying mechanism responsible for the unique dynamic ON-resistance behavior is unified by demonstrating the presence of critical drain stress voltage, above which dynamic ON-resistance increases significantly, in different gate stacks. Metal–insulator–semiconductor (MIS)- and Schottky-gated HEMTs show similar dependence of critical voltage on various parameters, which establishes that gate-stack design has negligible impact on the observed phenomena. Furthermore, using the physical insights developed, this work proposes a novel surface passivation scheme to improve the dynamic performance of the device. The proposed surface passivation scheme uses p-type $Al_{0.5}Ti_{0.5}O$ (AlTiO), which is deposited over SiN_x passivation (or GaN cap), and is shown to be an effective tool in improving the dynamic ON-resistance of the device by modulating the electric field in the GaN buffer. The proposed passivation scheme has avoided the critical voltage to appear for the entire drain stress voltage, stress time, and substrate bias range. Detailed computational analysis in conjunction with electroluminescence (EL) and photoluminescence (PL) studies revealed an electric field redistribution due to the p-type nature of AlTiO deposited over the surface passivation/capping layer, which is responsible for relaxed electric field profile in GaN buffer and observed improvement in dynamic performance. Besides, the new observations have further helped to understand the interplay between surface conditions and GaN buffer, defining its collective role in governing the dynamic performance of GaN HEMTs. Finally, various findings and the proposal in this work have been validated for buffers having higher carbon doping and devices with p-type AlTiO deposited over GaN cap instead of *in situ* SiN_x cap.**

***Index Terms*— AlGaN/GaN HEMTs, AlTiO, carbon-doped buffer, device design, dynamic ON-resistance, surface passivation.**

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I. Introduction

INTENTIONAL doping of GaN buffer by carbon to reduce leakage and improve breakdown [1], [2] has also emerged as a major source of dynamic ON-resistance (R_{ON}) in the AlGaN/GaN HEMTs [3]–[5]. Surface passivation, on the other hand, has evolved as a key approach to improve the dynamic R_{ON} of the devices [6]–[19]. Different approaches, e.g., plasma-enhanced chemical vapor deposition (PECVD) SiN_x [7], AlN [8]–[10], AlN/SiN_x stack [11], GaN cap [14], NH_3 plasma surface treatment [15], and low pressure chemical vapor deposition (LPCVD) SiN_x [12], [13] have been reported as effective surface passivation techniques to improve the dynamic R_{ON} performance of AlGaN/GaN HEMTs. Although the proposed surface passivation schemes have addressed the dynamic R_{ON} phenomena, previous works did not validate its applicability for extreme scenarios like longer stress times, lower temperatures, higher current injection, and higher electric field caused by various design parameters, which can lead to the presence of a critical drain stress voltage and a significant increase in dynamic R_{ON}, as reported in part I of this work [20]. Moreover, the physical phenomena involved in dynamic performance improvement with surface passivation are not completely understood. Although conventional understanding suggests passivation of surface traps to be responsible for this improvement, recent studies [16], [17] suggest a more complex physical phenomena involved, wherein surface passivation affects buffer trap dynamics. Detailed physical insights explaining the interplay between surface and buffer trap dynamics, which collectively governs the dynamic ON-resistance behavior of HEMTs is, therefore, missing in previous works.

In this work, we analyze the impact of gate-stack and surface passivation on the dynamic performance of the device under different stress conditions. Based on the improved understanding of the physical process involved in determining the dynamic performance of the device, a novel surface passivation scheme is proposed and demonstrated. The proposed surface passivation scheme improved the dynamic R_{ON} performance of the HEMTs, independent of the GaN buffer stack. This work is arranged as follows: details of HEMT fabrication and the dynamic R_{ON} measurement routine followed for this

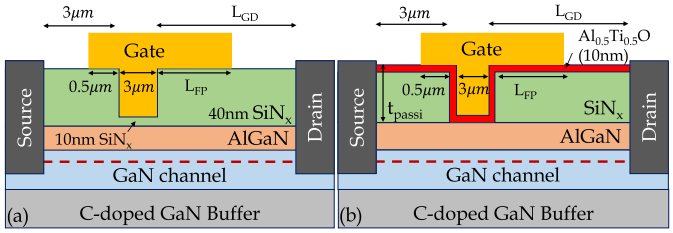

Fig. 1. Schematic of the fabricated (a) SiN_x-gated and (b) $Al_{0.5}Ti_{0.5}O$-gated AlGaN/GaN MISHEMTs showing the device parameters: gate–drain distance (L_{GD}), field plate length (L_{FP}), passivation thickness (t_{passi}); which vary for this work. The AlTiO-gated HEMTs have a 10-nm AlTiO deposited over SiN_x as passivation unlike the SiN_x-gated HEMTs with only SiN_x as passivation.

work is discussed in Section II. In Section III, the impact of gate-stack and surface passivation on the dynamic R_{ON} performance of GaN HEMTs as a function of various design parameters, gate–drain distance (L_{GD}), field plate length (L_{FP}), and passivation thickness (t_{passi}) is discussed. In order to understand the role of gate-stack, the dynamic performance of the metal–insulator–semiconductor (MIS)-HEMTs is compared with Schottky-gated HEMTs. A novel $Al_{0.5}Ti_{0.5}O/SiN_x$-based passivation scheme is proposed to improve the dynamic R_{ON}. The physical mechanism behind the improved dynamic R_{ON} is then explained in Section IV. In Section V, the effectiveness of $Al_{0.5}Ti_{0.5}O/SiN_x$ as passivation for HEMTs with different C-doped GaN buffer is discussed, post which the work is concluded in Section VI.

II. Device Fabrication and Experimentation

A well-optimized process, as reported in our earlier work [21], was used to realize AlGaN/GaN HEMTs on a 6" (commercial grade) C-doped GaN on Si epi-stack (Stack 1). The process starts with a Ti-based ohmic contact formation followed by mesa isolation using Cl_2 based dry etching. In order to study the impact of gate-stack on the dynamic R_{ON} of the GaN HEMTs, MISHEMTs have been processed. Ni/Au gate was deposited on 10 nm SiN_x dielectric to demonstrate SiN_x-gated MISHEMTs, as shown in Fig. 1(a). The gate electrode was extended above a thicker SiN_x (SiN) passivation to form field plate (FP) structures. Besides SiN_x gate, 10 nm $Al_{0.5}Ti_{0.5}O$ (AlTiO)-gated HEMTs, as shown in Fig. 1(b), were also fabricated by depositing the gate oxide using thermal atomic layer deposition (ALD), discussed in detail in our previous work [21]. In order to study the role of surface passivation on the HEMT dynamic performance, the MISHEMTs were passivated with 10 nm $Al_{0.5}Ti_{0.5}O$ (AlTiO) deposited on top of SiN in the access regions before evaporation of the FP metal, as shown in Fig. 1(b). The HEMT design parameters, viz. L_{GD}, L_{FP}, and t_{passi}, were also varied across the test chip to study their role on dynamic R_{ON} of the device. It is worth highlighting here that the HEMTs were processed using a well-optimized process [21] under similar process conditions and surface cleaning to minimize any process-related variability across the devices.

Fig. 2(a) depicts the transfer characteristics (I_D–V_{GS}) of the fabricated MISHEMTs. While SiN-gated HEMTs showed typical depletion mode operation with a deep-seated threshold voltage (V_{TH}) of −7 V, $Al_{0.5}Ti_{0.5}O$-based HEMTs showed a significant positive shift in V_{TH} (≈ −1 V) due to the p-type nature of the gate oxide [21]. The p-type oxide, however, achieved this positive V_{TH} shift while retaining the other HEMT performance metrices at par with the best reports till date [21]. This can be seen from Fig. 2(a), which shows excellent ON and OFF-state performance of the fabricated HEMTs with negligible I_D–V_{GS} hysteresis, irrespective of the gate oxide. The output characteristics (I_D–V_{DS}) of the fabricated MISHEMTs, as seen from Fig. 2(b), also shows both the HEMTs to have a similar ON-current (≈400 mA/mm) and pristine R_{ON}. The gate leakage (I_G–V_{GS}) of both AlTiO- and SiN-gated HEMTs, as depicted in Fig. 2(c), shows very low leakage in inversion region. However, in the accumulation region, there is a significant increase in leakage for the SiN-gated HEMTs. This is attributed to the low conduction band offset between AlGaN and SiN [22]–[24]. Moreover, in order to study the effectiveness of the proposed AlTiO-based surface passivation scheme, Schottky and $Al_{0.5}Ti_{0.5}O$-gated HEMTs were also processed over HEMT stack having GaN buffer with higher C-doping than Stack 1 (Stack 2).

Dynamic R_{ON} (ΔR_{ON}) for the MISHEMTs was evaluated by stressing the device [17] for 100 μs in OFF-state immediately followed by an I_D–V_{DS} sweep at $V_{GS} = 1$ V. In some cases, the devices were also subjected to longer stress times to probe the stress time dependence of ΔR_{ON}. The OFF-state stress was realized by biasing the HEMT using 26XX SMUs at $V_{GS-Stress} = V_{TH}-2$ V and OFF-state drain stress voltage ($V_{DS-Stress}$) varied from 0 to 200 V. Here, ΔR_{ON} was evaluated as follows:

$$\Delta R_{ON}\ (\text{in } \%) = \frac{R_{Post-Stress} - R_{Pristine}}{R_{Pristine}} \times 100 \qquad (1)$$

where $R_{Pristine}$ and $R_{Post-Stress}$ is the HEMT's R_{ON} in pristine and post stress conditions, respectively. The R_{ON} is measured from inverse slope of I_D–V_{DS} for $V_{DS} = 0.25$ to 0.5 V. Fig. 2(d) shows a typical I_D–V_{DS} characteristics of the MISHEMTs obtained during the measurement routine. It shows a significant $V_{DS-Stress}$ dependent increase in R_{ON}, which results in an observable ΔR_{ON} in the SiN-gated HEMTs. No such degradation was however, observed in the AlTiO-gated HEMTs, as seen from Fig. 2(b). Besides, the measurement routine also included a 180 s recovery time to recover the MISHEMTs to pristine condition after measuring $R_{Post-Stress}$ and before the next stress cycle, as depicted in Fig. 2(d).

III. Impact of Gate-Stack and Novel Surface Passivation

A. Gate-Stack Design

The dynamic performance of Schottky-gated GaN HEMTs with C-doped buffer, dealt in Part I of this work [20], revealed a critical $V_{DS-Stress}$ (V_{cr}) beyond which the ΔR_{ON} of the HEMTs degraded significantly. It is important to understand the role of gate-stack on the dynamic performance of the HEMTs, especially because GaN MISHEMTs have recently gained much prominence due to lower gate leakage and higher

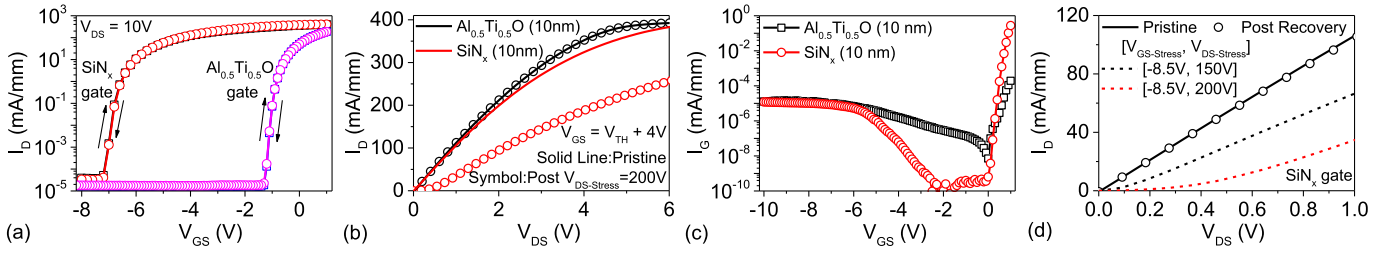

Fig. 2. (a) Dual sweep transfer (I_D–V_{GS}) characteristics, (b) output (I_D–V_{DS}) characteristics, and (c) gate leakage (I_G–V_{GS}) characteristics of the fabricated $Al_{0.5}Ti_{0.5}O$- and SiN_x-gated HEMTs depicting superior HEMT performance. The R_{ON} of the $Al_{0.5}Ti_{0.5}O$- and SiN_x-gated HEMTs was 8.9 Ω-mm and 9.4 Ω-mm, respectively. (b) Also shows a significant increase in R_{ON} post a $V_{DS-Stress}$ of 200 V for 100 μs in the SiN_x-gated HEMTs, while no such degradation was observed for the $Al_{0.5}Ti_{0.5}O$-gated HEMTs with similar pristine R_{ON}. (d) Typical I_D–V_{DS} characteristic of the SiN_x-gated HEMTs for $V_{GS} = 1$ V, obtained during the dynamic R_{ON} measurement routine. Devices show significant increase in ON-resistance as a function of OFF-state stress ($V_{DS-Stress}$). The devices recovered to pristine condition after 180 s recovery post the stress, as seen from the overlapping I_D–V_{DS} characteristics with the pristine HEMT.

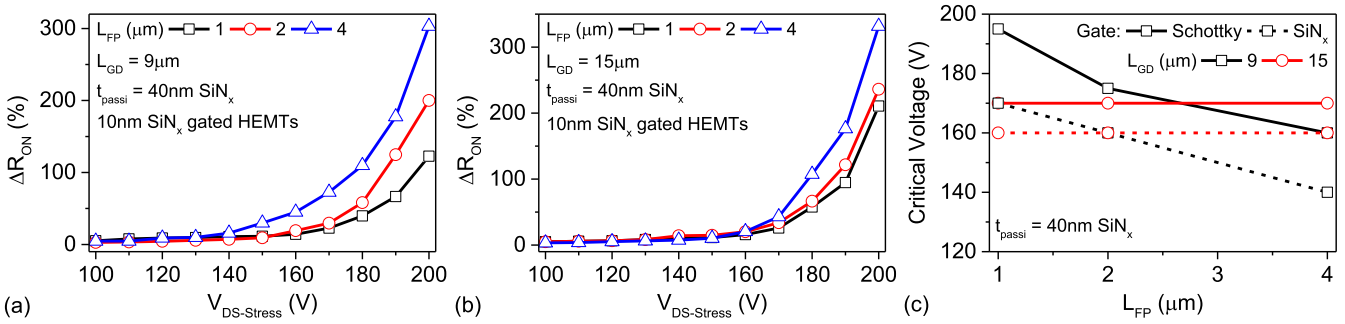

Fig. 3. Dynamic R_{ON} for SiN_x-gated GaN HEMTs as a function of lateral device parameter: field plate length (L_{FP}) for gate–drain distance (L_{GD}) of (a) 9 μm and (b) 15 μm showing a device parameter dependent critical voltage (V_{cr}) in the HEMTs. (c) Similar dependence of critical voltage on the device design parameters: L_{FP} and L_{GD} for both the Schottky and SiN_x-gated GaN HEMTs on C-doped buffer. Both Schottky- and MIS-HEMTs had a 40-nm SiN_x passivation ($t_{passi} = 40$ nm). Besides, V_{cr} is defined as the $V_{DS-Stress}$ for which $\Delta R_{ON} > 10\%$.

gate overdrive. In order to analyze the impact of gate-stack, SiN-gated MISHEMTs were fabricated on the same C-doped GaN buffer as the Schottky HEMTs.

Dynamic performance of the SiN-gated devices as a function of $V_{DS-Stress}$ is shown in Fig. 3. Fig. 3(a) and (b) shows a V_{cr} beyond which the ΔR_{ON} degrades significantly for the GaN MISHEMTs too. Fig. 3(a) also shows the V_{cr} to be dependent on L_{FP} in the SiN-gated HEMTs. V_{cr} for the HEMTs with $L_{GD} = 9$ μm is seen to reduce from ∼170 to ∼140 V as L_{FP} is increased from 1 to 4 μm. The V_{cr} however, shows reduced dependence on L_{FP} for larger L_{GD} (15 μm), as seen in Fig. 3(b). Besides, the MISHEMTs with larger L_{FP} also showed a higher ΔR_{ON} for $V_{DS-Stress} > V_{cr}$.

Fig. 3(c) summarizes the dependence of V_{cr} on L_{GD} and L_{FP} for the SiN-gated HEMTs and compares it with the Schottky-gated HEMTs, discussed in Part I of this work [20]. Fig. 3(c) shows a similar dependence of V_{cr} on L_{FP} and L_{GD} for the HEMTs, irrespective of them being Schottky- or MIS-gated. The V_{cr} for both the Schottky- and MIS-gated HEMTs with $L_{GD} = 9$ μm, is seen to reduce as the L_{FP} is increased from 1 to 4 μm. Besides, both the HEMTs show a reduced dependence of V_{cr} on L_{FP} for $L_{GD} = 15$ μm. It is worth highlighting here that both the HEMTs, which demonstrated this similar dependence of V_{cr} on L_{GD} and L_{FP}, had 40 nm SiN as passivation with the only difference being

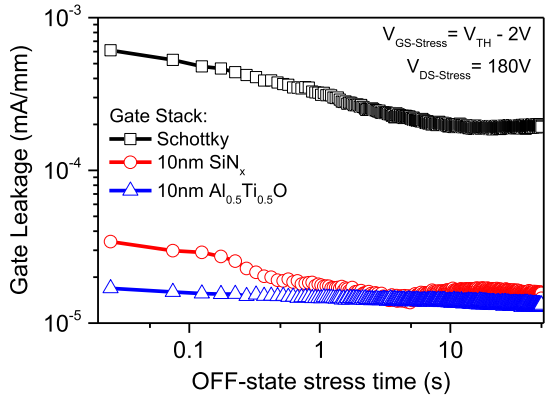

Fig. 4. Gate leakage during OFF-state stress for Schottky, 10 nm SiN_x and 10 nm $Al_{0.5}Ti_{0.5}O$ gated HEMTs. The gate leakage in Schottky-gated HEMTs under OFF-state is ∼20× greater than the MISHEMTs.

in the gate-stack. Besides, similar behavior was observed in spite of a ∼ 20× higher OFF-state gate leakage in the Schottky HEMTs as compared to the SiN HEMTs, as seen in Fig. 4. These observations confirm negligible impact of gate-stack and gate leakage on the V_{cr} as well as ΔR_{ON} behavior of C-doped GaN HEMTs. Rather, similar dependence of V_{cr} on

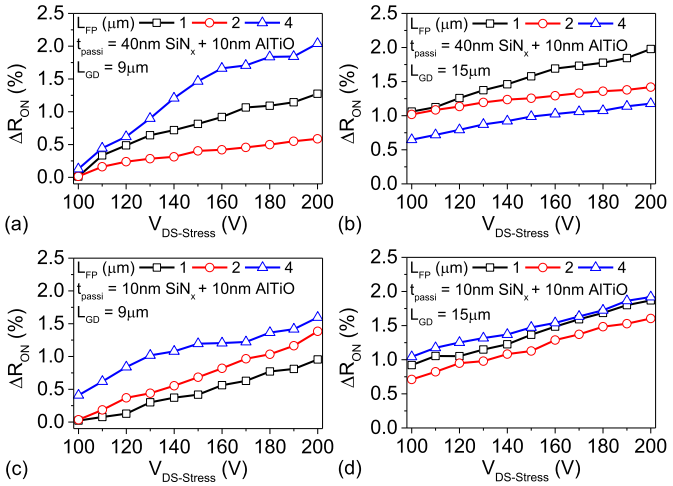

Fig. 5. Dynamic R_{ON} of MISHEMTs, with 10 nm $Al_{0.5}Ti_{0.5}O$ deposited on top of SiN_x (AlTiO/SiN passivation), as a function of field plate length (L_{FP}) for gate–drain distance (L_{GD}) of (a), (c) 9 μm, and (b) and (d) 15 μm. HEMTs have AlTiO deposited on top of (a) and (b) 40 nm SiN_x and (c) and (d) 10 nm SiN_x passivation, respectively. The dynamic R_{ON} for these HEMTs did not show any critical voltage till 200 V. Moreover, any dependence on L_{FP}, L_{GD} and thickness of SiN_x under AlTiO layer was also found to be missing.

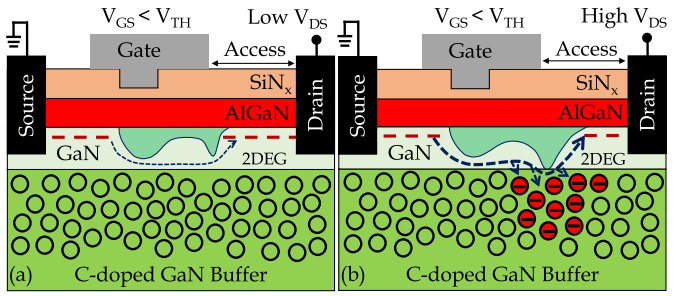

Fig. 6. Device schematic depicting the electron trapping phenomena leading to observed ΔR_{ON} characteristics of HEMTs with SiN_x passivation. (a) Represents the condition in which applied $V_{DS-Stress}$ is small enough to prevent carrier injection into the GaN buffer. This is supported by a lower ionization probability of buffer traps due to lower field across the GaN stack, which leads to negligible ΔR_{ON}. (b) Represents the condition in which applied $V_{DS-Stress}$ is high enough to cause sufficient carrier injection which combined with increased buffer trap ionization probability at higher electric fields results in significant ΔR_{ON}. The estimated electron path is represented by a dashed line with linewidth representing the magnitude of leakage current.

L_{GD} and L_{FP} for the Schottky as well as MIS gated HEMTs establishes that the V_{cr} is dependent on the channel electric field.

B. Surface Passivation

Different surface passivation schemes were also analyzed for their impact on ΔR_{ON} behavior of the device. While the devices discussed in Fig. 3 had SiN as surface passivation, a different passivation scheme with 10 nm $Al_{0.5}Ti_{0.5}O$ grown as surface protection layer over SiN passivation (AlTiO/SiN passivation), as seen in Fig. 1(b), is discussed in this section. As V_{cr} and ΔR_{ON} were found to have negligible dependence

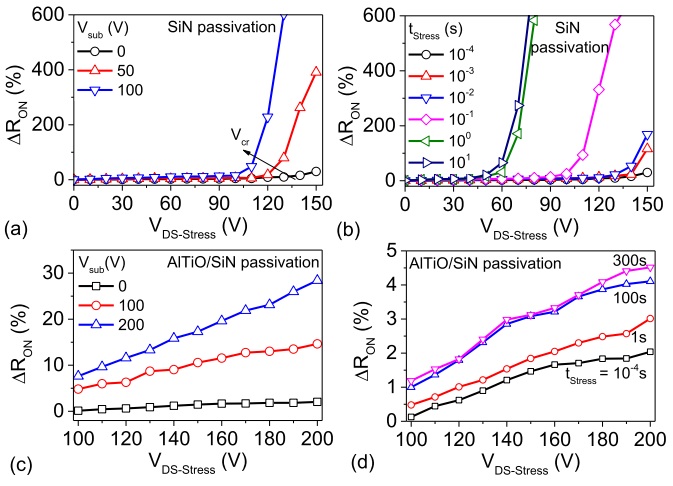

Fig. 7. Dynamic R_{ON} of the MISHEMTs as a function of (a), (c) substrate bias (V_{sub}), and (b) and (d) stress time (t_{Stress}). The Dynamic R_{ON} of MISHEMTs with only SiN passivation is shown in (a) and (b), while (c) and (d) show the performance of HEMTs with AlTiO deposited on top of SiN passivation. The HEMTs with only SiN passivation show a critical voltage (V_{cr}), beyond which the ΔR_{ON} increases significantly, to be a strongly dependent on V_{sub} and t_{Stress}. The HEMTs with AlTiO/SiN passivation however, showed low dynamic R_{ON} with no critical voltage till 200 V even for higher positive V_{sub} and longer t_{Stress}. Device dimension: $L_{GD} = 9$ μm and $L_{FP} = 4$ μm. SiN passivated HEMTs have 40 nm SiN, while AlTiO/SiN passivated HEMTs have $t_{passi} = 40$ nm $SiN_x + 10$ nm $Al_{0.5}Ti_{0.5}O$.

on gate-stack, these HEMTs also used AlTiO as the gate oxide for ease of processing.

Fig. 5 shows extremely low ΔR_{ON} in AlGaN/GaN HEMTs with AlTiO/SiN passivation. Fig. 5(a) and (b) shows no V_{cr} till 200 V in the AlTiO/SiN passivated HEMTs, even for larger L_{GD} or L_{FP}, unlike the HEMTs with only SiN passivation as seen in Fig. 3. It should also be noted that the demonstrated improvement in ΔR_{ON} was achieved despite similar gate leakage seen in both SiN and AlTiO gated HEMTs, as seen in Fig. 4. This further validates the V_{cr} to be a gate-stack independent phenomenon.

Furthermore, HEMTs with 10 nm $Al_{0.5}Ti_{0.5}O$ deposited over a thinner SiN passivation, also did not show any V_{cr} till 200 V. This improvement was independent of L_{GD} and L_{FP}, as depicted in Fig. 5(c) and (d). These observations clearly establish AlTiO/SiN as a promising surface passivation scheme for improving the ΔR_{ON} behavior of C-doped AlGaN/GaN HEMTs. Given the fact that the observed ΔR_{ON} and V_{cr} in these devices were due to trapping of electrons in the acceptor traps introduced by C-doping in GaN buffer (discussed in part I of this work [20]), improvement in buffer induced ΔR_{ON} degradation by surface modification signifies a complex surface-buffer interplay in these HEMTs.

IV. Mechanism Responsible for Dynamic R_{ON} Improvement

A. Observations From Carrier Trapping Dynamics

The mechanism governing the presence of a V_{cr} in ΔR_{ON} of AlGaN/GaN HEMTs was proposed and justified in Part-I

of this work [20], which is summarized in Fig. 6. As per the proposed mechanism, V_{cr} was found to be due to the presence of a critical electric field in the access region and associated buffer trap ionization as well as carrier trapping. It was found to be a strong function of stress duration, carriers injected into GaN buffer, buffer trap ionization probability, electric field strength, substrate bias, and temperature. Externally increasing the carrier injection in the GaN buffer and carrier trapping by increasing positive substrate bias voltage (V_{sub}) and stress duration (t_{Stress}) was found to drastically reduce V_{cr} of the device. This validated the proposed phenomena and provided a method to externally modulate the V_{cr} of the device. Such a reduction in V_{cr} with increasing positive V_{sub} and t_{Stress} was also observed in the SiN-gated HEMTs with SiN passivation, as seen in Fig. 7(a) and (b), respectively.

Devices with AlTiO/SiN surface passivation were also studied to investigate dependence of its dynamic performance on stress time and carrier injection into the GaN buffer. For higher V_{sub} and t_{Stress}, a much lower V_{cr} is expected. Fig. 7(c) and (d) show the impact of V_{sub} and t_{Stress} on ΔR_{ON} of the device. It can be observed from Fig. 7(c) that though the ΔR_{ON} increases when carrier injection into GaN buffer was increased by applying positive V_{sub}, V_{cr} was not observed for these devices up to stress voltage of 200 V despite applying a very high V_{sub} of 200 V. Similarly, Fig. 7(d) shows the absence of V_{cr} for devices with AlTiO/SiN as surface passivation even for stress time as high as 300 s. However, devices with only SiN_x surface passivation, as seen in Fig. 7(b) and discussed in Part I of this work [20], had a significantly reduced V_{cr} when stress time was increased from 100 μs to 10 s. Furthermore, it should be noted that a reduction in V_{cr} for higher positively applied V_{sub}, as seen in Fig. 7(a) and discussed in Part I of this work [20], indicates increased buffer trapping in these devices as V_{sub} increases carrier injection in the GaN buffer. However, the same seems to be missing/relaxed in devices with proposed AlTiO/SiN surface passivation scheme. This is confirmed in Fig. 8, which shows missing carrier trapping (i.e., no change in source current with respect to time) in AlTiO/SiN passivated devices when compared to SiN passivated devices, which show significant presence of carrier trapping (i.e., drop in source current as a function of time).

B. Impact of Surface Passivation on Electric Field

As devices with AlTiO/SiN passivation show a lower source-drain leakage current as compared to SiN passivated devices, as seen in Fig. 8, it suggests a reduction in electric field magnitude in the channel. Furthermore, the absence of V_{cr} even under application of very high V_{sub} and increased t_{Stress}, indicates reduced trap ionization probability under a given stress condition, which also suggests relaxation in trap ionization or electric field in the access region. In order to further analyze this aspect, a lateral electric field profile was analyzed using electroluminescence (EL) spectroscopy. Fig. 9(a) and (b) shows the EL line scans of the Schottky and SiN gated MISHEMTs along the gate–drain access

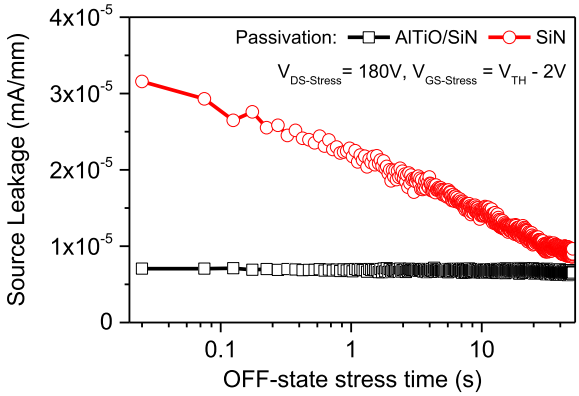

Fig. 8. OFF-state source current as a function of stress time for devices having SiN and AlTiO/SiN passivations. The device dimensions are: $L_{\text{GD}} = 15$ μm, $L_{\text{FP}} = 2$ μm.

region. Irrespective of the gate-stack, the EL line spectra of the GaN HEMTs show a similar electric field peaking near the FP edge followed by an exponential decay in the gate–drain access region. Fig. 9(c), depicting the EL line scan of AlTiO/SiN passivated HEMTs, however, shows that unlike SiN passivated MISHEMTs, the introduction of $Al_{0.5}Ti_{0.5}O$ significantly redistributes the electric field in the gate–drain access region with no field peak near the FP edge. Field relaxation and lower OFF-state source current combined with the observations from Section IV-A establish relaxed trap ionization and carrier trapping to be responsible for improved dynamic performance of the AlTiO/SiN passivated devices.

C. Why AlTiO-Based Passivation Scheme Improved Dynamic R_{ON} Performance?

In Section II-B, modulation of lateral electric field profile was found to be responsible for the improvement in the dynamic performance of the device. As both Schottky- and SiN-gated HEMTs have similar electric field profiles [Fig. 9(a) and (b)], the HEMTs showed similar dependence of V_{cr} on the device parameters [Fig. 3(c)]. On the other hand, while EL line scans show a relaxation in the electric field near the FP edge with AlTiO/SiN surface passivation, it was difficult to experimentally evaluate its impact on the source-drain leakage current. In order to further analyze the effect, TCAD based analysis was carried out on devices with AlTiO/SiN as surface passivation layer using a well-calibrated TCAD framework [2], [25]. Since AlTiO is found to be a p-type oxide with Al% controlling its p-type property, which we confirmed using Hall measurements [21], the doping in AlTiO was modeled as shallow acceptor traps with an activation energy of $E_V + 0.1$eV. It should be noted that since the activation energy is not experimentally known, a lower value was selected so as to ensure ionization of acceptor states to contribute holes in AlTiO under thermal equilibrium, which corroborates with experimentally measured value [21]. Fig. 10 compares the electric field profile as a function of acceptor trap concentration in AlTiO. It shows a field redistribution in

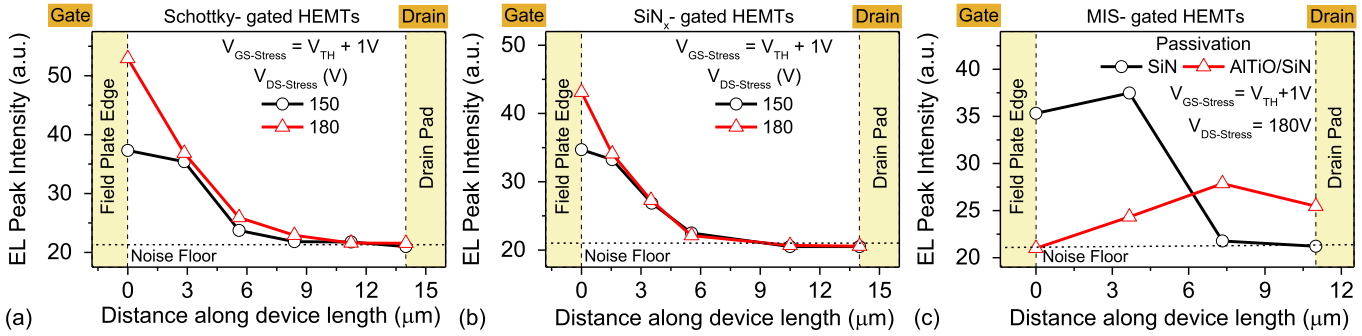

Fig. 9. EL intensity line scans along gate–drain access regions of (a) Schottky-gated and (b) SiN_x-gated HEMTs showing similar electric field profile for both the HEMTs, with the EL intensity peaking near the field plate edge. The device dimensions are: $L_{GD} = 15$ μm, $L_{FP} = 1$ μm and SiN_x passivation thickness of 40 nm. (c) EL line scans along gate–drain access regions of HEMTs with AlTiO/SiN passivation showing redistributed electric field with no field peak at field plate edge, unlike HEMTs with only SiN_x passivation. The device parameters are: $L_{GD} = 15$ μm and $L_{FP} = 4$ μm.

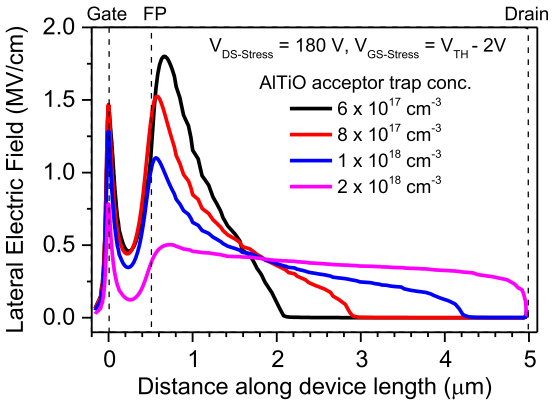

Fig. 10. Lateral electric field in HEMTs with AlTiO/SiN surface passivation showing redistributed electric field profile with reduced peak at gate edge and field plate edge as acceptor traps in AlTiO is increased. These acceptor traps are introduced in the AlTiO due to their p-type nature.

the gate–drain access region with an increase in acceptor trap concentration or Al doping. This field redistribution results in a field relaxation near the gate edge as well as an FP edge, similar to the EL line scan extracted field profile shown in Fig. 9(c). Reduction in peak field value will drastically reduce the trap ionization probability and hence, increase V_{cr}. Additionally, the resulting current contours shown in Fig. 11 depicts a reduction in carrier injection into the buffer as p-type doping concentration, represented by acceptor states density in AlTiO, is increased.

The above observations establish that reduced trap ionization probability due to efficient field redistribution and reduced carrier injection into GaN buffer results in the observed improvement in the dynamic performance of the device with AlTiO/SiN as surface passivation. Furthermore, field relaxation by the proposed surface passivation ensures the negligible impact of L_{GD} and L_{FP} on the dynamic performance of the device as seen in Fig. 5. A similar argument holds true for the absence of V_{cr} even with higher V_{sub} of 200 V and higher t_{Stress} of 300 s, as seen in Fig. 7(c) and (d), respectively. The above arguments strongly suggest AlTiO surface protection-induced field relaxation be responsible for the observed improvement in the dynamic performance of the device. It should, however, also be noted that a possibility of AlTiO surface passivation scheme shifting the detrapping time constant outside the poststress measurement window, i.e., to submicroseconds time scales, cannot be completely ruled out.

These findings further help to understand the interplay between surface and buffer conditions, which was also highlighted in our recent works [26], [27]. In part-I we noticed that as far as surface conditions do not change the electric field profile in the buffer region, dynamic ON-resistance was independent of surface conditions/leakage [20]. However, if surface conditions modulate the electric field in the GaN buffer, as observed in this work, the dynamic behavior of GaN HEMT is affected accordingly.

V. Independence of C-Doping in GaN Buffer

To establish the proposed technique as a promising approach for improving the dynamic performance of the device, the performance of the proposed surface passivation scheme was further examined on a different epi-stack having a higher C-doping concentration (Stack 2). High C-doping in Stack 2 has been verified using the photoluminescence (PL) spectra of the stack using a 325 nm laser, as shown in Fig. 12. The PL spectra of Stack 2 show a broad luminescence in the yellow luminescence (YL) and blue luminescence (BL) band, which is attributed to the C-doping induced acceptor traps in the GaN buffer [28], [29]. Furthermore, Fig. 12 shows the presence of a strong BL in Stack 2 unlike in Stack 1, which is due to a higher C-doping in Stack 2, as reported in [28]. Fig. 13 shows the ΔR_{ON} performance of the HEMTs on Stack 2. In the case of the device without AlTiO over GaN cap, V_{cr} was found to be as low as 50 V due to very high C-doping in the GaN buffer. On the other hand, devices with AlTiO passivation did not show V_{cr} for the measured range. This establishes surface protection of SiN passivation or GaN cap by deposition of AlTiO, as a novel passivation scheme, to mitigate ΔR_{ON} in GaN HEMTs, irrespective of the doping in GaN buffer.

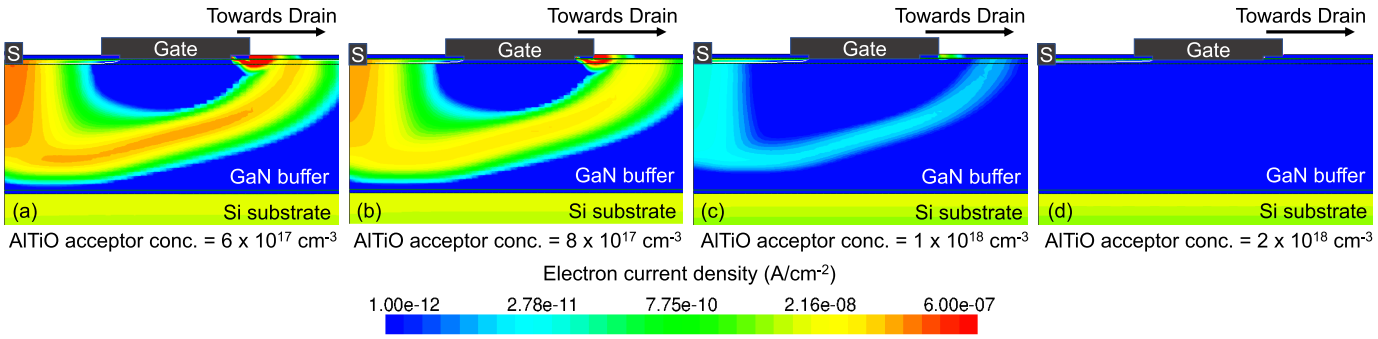

Fig. 11. Current density contours extracted for a AlTiO/SiN passivated HEMT with acceptor trap concentrations of (a) 6×10^{17} cm^{-3}, (b) 8×10^{17} cm^{-3}, (c) 1×10^{18} cm^{-3}, and (d) 2×10^{18} cm^{-3} in AlTiO. The contours depict a reduction in leakage current through the GaN buffer as the acceptor trap concentration in the passivation is increased. The contours were extracted at a $V_{DS-Stress}$ of 200 V and $V_{GS-Stress} = V_{TH} - 2$V while keeping a shorter L_{GD} (= 5 μm) to account for the worst case.

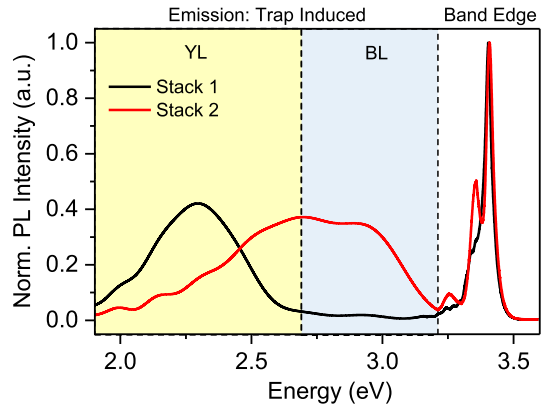

Fig. 12. PL spectra of C-doped GaN buffers: Stack 1 and Stack 2 using a 325 nm laser. BL and YL peaks due to C-doping induced buffer traps shows higher C-doping in Stack 2 as compared to Stack 1.

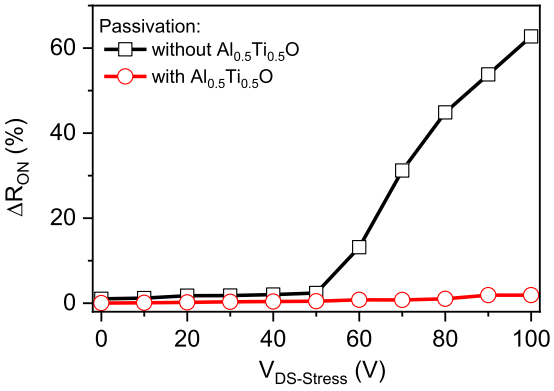

Fig. 13. Dynamic R_{ON} of HEMTs with and without $Al_{0.5}Ti_{0.5}O$ protection layer over GaN cap as surface passivation scheme. The HEMTs have a GaN buffer with high C-doping (Stack 2). Unlike the devices with conventional passivation, HEMTs with AlTiO deposited over GaN cap did not show any critical voltage.

VI. Conclusion

Dependence of dynamic ON-resistance in AlGaN/GaN HEMTs with C-doped buffer on gate-stack and surface passivation was studied. Gate-stack design was found to have a negligible impact on the HEMT's dynamic ON-resistance. Both SiN_x and Schottky-gated HEMTs depicted very similar dynamic behavior, i.e., both depicted the presence of a critical drain stress voltage above which signature of carrier trapping in GaN buffer was observed and HEMT's dynamic ON-resistance increased significantly. To mitigate this phenomenon, p-type $Al_{0.5}Ti_{0.5}O$ was introduced on top of SiN_x passivation and GaN capping layer. In the presence of an AlTiO-based novel passivation scheme, dynamic ON-resistance was found to be missing with no critical voltage observed for the entire measurement range. The effectiveness of the passivation scheme was established even under conditions that would reduce the critical voltage such as longer stress times, positive substrate bias, and higher C-doping in the buffer. This was attributed to the redistribution of the electric field across the entire access region with a relaxed electric field near the gate/field plate edge, which was earlier localized at the gate and field plate edge. These findings further help to understand the interplay between surface conditions and buffer. In part-I, we noticed that as far as surface conditions do not change the electric field profile in the buffer region, dynamic ON-resistance was independent of surface conditions/leakage. However, if surface conditions modulate the electric field in the GaN buffer, the dynamic behavior of GaN HEMT is affected accordingly, as observed in this work. Redistribution of lateral electric field and reduced electric field strength near field plate edge mitigated the possibility of electron trapping in the acceptor traps of GaN buffer, which resulted in the improved dynamic performance of C-doped AlGaN/GaN HEMTs.

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