Record Low Metal – (CVD) Graphene Contact Resistance Using Atomic Orbital Overlap Engineering

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Abstract — In this work, for the first time, different techniques to strengthen atomic orbital overlap are proposed to engineer metal – graphene contact, while highlighting relevance of sp-hybridized carbon atoms in the contact region. The fundamental understanding of contact's quantum chemistry has resulted in record low contact resistance for CVD graphene when compared with the best reported till date for CVD as well as epitaxial graphene – metal contacts. Role of contact engineering in terms of reaching graphene FET's intrinsic limits with scalability is presented in detail. Finally, record high transistor performance is demonstrated as a result of engineered contacts.

I. Introduction

After over a decade research on graphene, there is no doubt about graphene's fascinating electrical, mechanical & thermal properties, and most importantly its capability to enable THz technologies (Fig. 1). However, as depicted in Fig. 1, attributed to technological limitations like gate and substrate dielectric, origin of graphene monolayer and contact resistance, graphene FET's RF characteristics can be significantly better or worst. In this direction, graphene – metal contact resistance plays a crucial role and is considered to be the performance killer [1]. For example, it was predicted that graphene's intrinsic cut-off frequency (F_t) can be as high as 7 THz at the channel length (L_G) of 10nm if contacts are transparent [2], however, the same can drop down to sub-THz range with a finite contact resistance [3][4]. So far a number of groups have reported a range of metal – graphene contact resistance values using a variety of metals (Fig. 2). High metal – graphene contact resistance at room temperature has been often attributed to limited Density of States of graphene near Dirac point, metal – graphene work-function difference, sandwiched impurities at the metal – graphene interface, channel and substrate quality, wettability, process conditions and metal stack used [5] – [12]. Recently we presented that metal – graphene contact depends on orbital overlap (hybridization) between carbon and metal atom [12]. This work while validating the quantum chemistry of contacts, experimentally demonstrates record low contact resistance for metal graphene interface at room temperature.

II. Quantum Chemistry of Contacts

Graphene has sp-hybridized carbon atoms at its edge, whereas sp^2-hybridized atoms in the overlap region; both form a contact with metal (Fig. 3). Though sp^2–hybridized sites are neutral in terms of bonding with metal atoms, sp–hybridized carbon atom, with an unhybridized p orbital forms a bonding channel with metal atom by hybridizing (i.e. orbital overlap) with its d orbital [13]. This is evident from the Mulliken charge population depicting a substantial charge transfer of the order of ~0.1e per C atom from Palladium to carbon at the Edge region; however, the same in the overlap region is ~0.06e per C atom (Fig. 4). The same for Pt atoms at the edge region is 0.05e per C atom. This contributes to 40% of the total current conduction through sp-hybridized atoms when compared to sp^2-hybridized sites in the graphene - metal (Pd) overlap region (Fig. 5).

III. Atomic Orbital Overlap Engineering

The chemical role of sp-hybridized carbon atoms at the edge suggests that increasing the sp-hybridized carbon atoms can potentially improve the contact resistance. The missing orbital overlap in the metal – graphene overlap region is attributed to the inability of sp^2-hybridized carbon atoms to form a chemical covalent bond with the metal atoms. To increase the orbital overlap or bonding channels, novel contact geometries by introduction of defect in the overlap region using chemical or physical means (Fig. 5a) are proposed in this work. In addition to this lithographically patterned edges in the metal – graphene overlap region are formed to increase edge perimeter per unit device width (Fig. 5b). Ab-initio calculations depict that the proposed approach increases number of transport channels between metal – graphene due to strong orbital overlap between palladium atoms and sp-hybridized carbon atoms (Fig. 6a) without affecting transport properties of the channel (Fig. 6b).

IV. Experimental Approach

Three methods are proposed and demonstrated to create sp–hybridized defects, as depicted in Fig. 7a, samples before metal deposition were exposed either to (i) controlled O_2 or Ar plasma or (ii) O_2 or Ar ion bombardment, in order to introduce sp–hybridized / defected graphene sites. In another technique an energetic electron beam with less than 5nm diameter was used to systematically introduce defects in the contact area. The electron beam was systematically scanned through the whole contact area with a finite step in x–y plane (Fig. 7b). Except ion bombardment technique, vacuum was broken after defect creation and before metal deposition. For TLM test structures (Fig. 8a), to study metal – graphene contact behavior and transistor characteristics, CVD grown monolayer graphene (on Cu) was transferred over Si/SiO_2 substrate using an optimized wet transfer process. Fig. 8b depicts lithographically patterned edges to increase edge perimeter. These are named "*Comb*" geometries, whereas the earlier are named "*Defect*" and "*ebeam*" geometries in this work. Furthermore, combinations of *Defect/ebeam* and *Comb* were also realized to validate role of tunneling component vs. transport through bonding channels.

V. Record Low Contact Resistance

It is worth highlighting that number of sp-hybridized carbon atoms are less than 0.1%, when compared to sp^2-hybridized atoms in conventional contact geometry. Attributed to 40% conduction through overlapped orbital or bonding channel, even a 0.5% increase in sp-hybridized carbon atoms can theoretically bring metal – graphene contact resistance to its intrinsic limits. This, using the methods proposed above, can be increased by either increasing plasma exposure time, edge perimeter, or a combination of both. Figure 9 validates the discussion above and shows significant reduction in contact

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resistance, in all cases, when plasma exposure time was increased. Beyond an optimum exposure time, contact resistance rolls back to higher values. As the exposure time increases, defect density increases systematically (Fig. 10), which brings the contact resistance down to record low values. However, as the plasma exposure time increases further, increased defect density leads to current crowding in the contact area, which increases the contact resistance. Similarly, when edge perimeter was increased systematically, record minimum contact resistance can be clearly seen, which is attributed to ~25× increment in sp-hybridized carbon atoms and enhanced atomic orbital overlap. The lithographically pattered edges in the contact area together with electron-beam induced defect show promise to lower the contact resistance further down (Fig. 9d). These finding also validate the discussion on transport through bonding channel at the edges and tunneling in the overlap region. In addition to the approaches discussed so far, O_2 and Ar ion bombardment was also used to physically introduce defects in the contact area. Both the methods also result in significant reduction in contact resistance when compared to the case without contact engineering (Fig. 11). In summary, record low contact resistance has been achieved by different contact engineering techniques. This with O_2 plasma exposure and *ebeam* are 78 Ω−μm and 87 Ω−μm, respectively, at room temperature. The same by Ar ion bombardment is 94 Ω−μm and by *ebeam* (process-1) is 84 Ω−μm, while using CVD graphene channel.

VI. Record High Transistor Performance

Beside contact resistance, increasing sp-hybridized sites either by increasing edge perimeter or by increasing defect density are found to significantly improve the channel mobility (Fig. 13−14). At shorter channel lengths, channel mobility is limited by contact resistance, which seriously degrades the transistor performance and limits its intrinsic capabilities. Fig. 15a depicts that the channel mobility significantly improves when contact resistance was lowered. Moreover, lowering contact resistance is found to reduce the transfer length, which signifies reduction of tunneling component with contact engineering (Fig. 15b). An ultra scaled transfer length show promise to scale contact dimensions down to sub-50nm, when contact resistance is scaled below 50 Ω−μm. Furthermore, Fig. 16(a) shows ON current to be independent of contact resistance at lower contact resistance, which however has a logarithmic dependence when the same is above 400 Ω−μm. This has helped pushing the transistor to a region in which ON current is limited by the channel length and the channel mobility. However, transconductance and I_{ON}/I_{Dirac} continues to improve as contact resistance is lowered (Fig. 16 b–c). An improved I_{ON}/I_{Dirac}, i.e. improved I_{ON} without significantly affecting I_{Dirac}, as well as higher transconductance, hint that the contact engineering approach proposed here doesn't dope the channel with excess carriers. This is a promising effect for ultra scaled transistor designs. Clearly these results show that lowering the contact resistance significantly improves channel transport properties and allows transistor to perform up to its intrinsic limits. $I_{DS} – V_{DS}$ characteristics (Fig. 17a) shows that lowering contact resistance offers path to increase transistor current density and drive transistor in saturation. A reduction in saturation voltage was found (probed using nanosecond pulse measurements, data not shown here), when contact resistance was lowered. In addition to ON current improvement, mobility roll-off with channel length scaling is mitigated (17b). This gives promise to scale the transistor channel length to take advantages of scaled dimensions, as depicted in Fig. 17(c). Without contact engineering, ON current was found to be limited, which doesn't significantly improve with the channel length. Attributed to the discussed trends above, devices with engineered contacts are found to offer 6× improvements in I_{ON}, 8× improvements in transconductance and 6× improvements in channel mobility (Fig. 18). These improvements due to contact engineering have lead to CVD graphene devices to offer record high transistor performance (Fig. 19), which is better than the best reported till date for epitaxial graphene on SiC substrate [13]. Finally, figure 20 compares contact resistance reported by various groups with results from this work. Clearly the atomic orbital overlap engineering approach has allowed graphene contacts and channel to reach to its intrinsic limits, independent of source (CVD vs. exfoliated) of the channel material.

VII. Conclusion

Proposed atomic orbital overlap engineering by introduction of sp-hybridized carbon sites in the metal – graphene overlap area has shown to significantly improve the metal – graphene contact properties. A variety of techniques to engineer the orbital overlap has been demonstrated. Engineered contact with improved orbital overlap offers record low contact resistance 84 Ω−μm at room temperature, which is 138% and 28% better than best reported till date while using CVD and epitaxial graphene, respectively. Moreover, graphene devices with engineered contact offer scalability to shorter channel lengths, without sacrificing the channel properties. This has allowed graphene transistors demonstrated in this work to achieve performance close to its intrinsic limits and has lead to 6× improvement in ON current, 8× improvements in transconductance and 6× improvement in channel mobility. Finally, beside record low contact resistance, engineered contact devices have shown record high transistor performance when compared with the best reported epitaxial graphene FET on SiC substrate.

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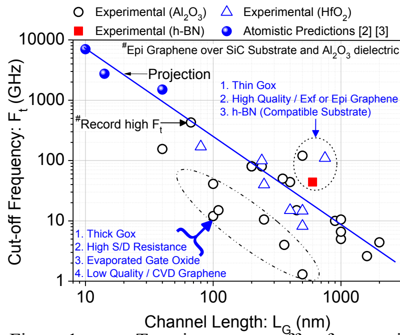


Fig. 1: Transistor cut-off frequencies experimentally reported or theoretically projected till date, in literature, as a function of channel length. Figure further depicts impact of technology parameters like gate oxide, gate oxide thickness, substrate and origin of graphene monolayer. Figure shows that the experimental trends are aligned with the simulated projection of 7 THz (f_t) at 10nm of channel length.

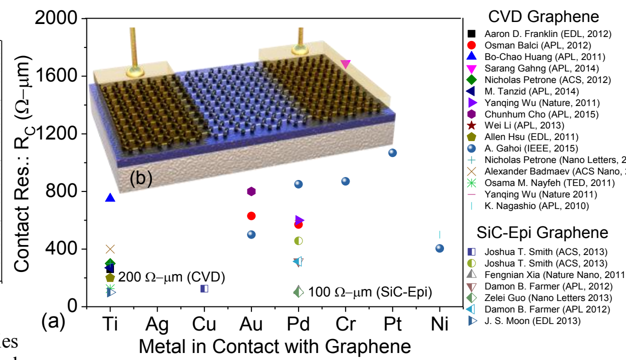


Fig. 2: (a) Contact resistance reported till date, by various groups, as a function of different contact metals, origin of graphene monolayer and substrate. Palladium and Titanium appears to offer least contact resistance with graphene. In case of Epi-grown graphene over SiC, lowest contact resistance till date is 100 Ω – µm, whereas the same for CVD grown graphene is 200 Ω – µm, till date. (b) Illustration depicting graphene – metal contact in a back gated FET.

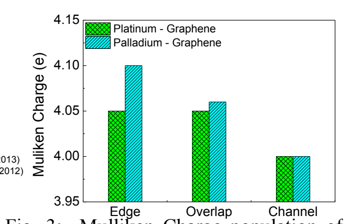


Fig. 3: Mulliken Charge population of Carbon atoms in the Edge, Overlap and Channel region of the graphene – metal interface. The charge transfer, per C atom from the metal atoms, calculated using DFT, depicts the strength of orbital overlap in a given region. For example in case of Palladium, such a high charge transfer from metal to graphene depicts presence of a strong hybridized state ($p_z - d_{z^2}$) at the graphene edge, which in case of Platinum contact and in the overlap region is missing.

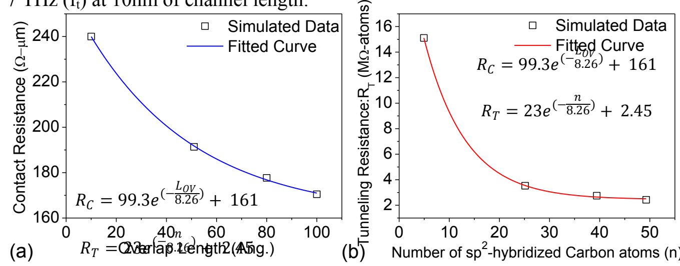


Fig. 4: (a) Calculated metal (Pd) – graphene contact resistance as a function of metal overlap length (L_{OV}). The calculated data is extrapolated to L_{OV} = 0 to find edge component (transport through sp–hybridized sites). (b) The tunneling component (transport through sp^2–hybridized sites) of total contact resistance saturates to 2.45 MΩ–atom, which attributes to an edge component of 1.58 KΩ – atom. Figure shows 40% current conduction through the edge region (through sp – hybridized carbon atoms), whereas 60% through overlap region (through sp^2 – hybridized carbon atoms) for $L_{OV} \rightarrow \infty$.

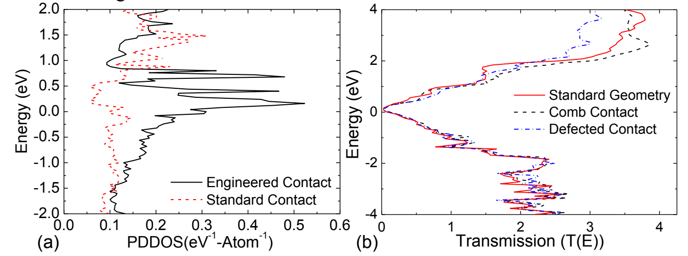


Fig. 6: (a) PDDOS of engineered vs. standard contact. Here engineered stands for contact with increased sp–hybridized sites. (b) Transmission spectrum of engineered vs. standard contact. An improved graphene PDDOS for engineered contacts, above Fermi energy, is attributed to strong atomic orbital overlap between carbon and with metal (Pd) atoms. However the same doesn't change in sp^2-hybridized regions due to lack of empty states for hybridization, which is evident from T(E). For first principle calculations ab-initio DFT and NEGF formalism is used, while using the local density approximation to describe the exchange-correlation interaction between the electrons.

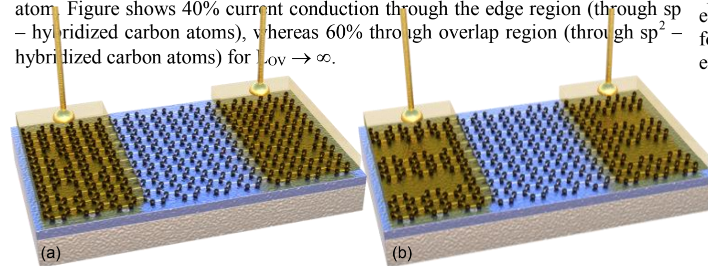


Fig. 5: Proposed engineered contacts with additional sp – hybridized carbon atoms in the metal–graphene overlap region by introducing (a) *Defects* and (b) lithographically patterning graphene to *Comb* like shapes. Note that the ratio of sp–hybridized sites to sp^2–hybridized sites, for L_{OV} = 200nm is just 1/1550 (0.065%), which means even a 0.4% increase in sp–hybridized sites, can lower the contact resistance by 4× or higher.

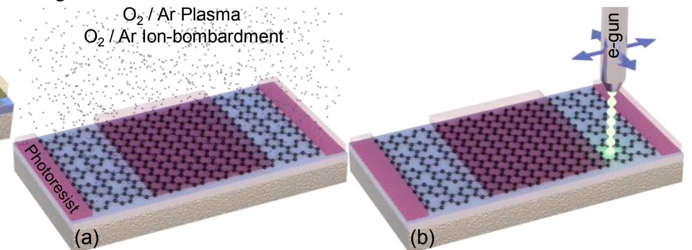
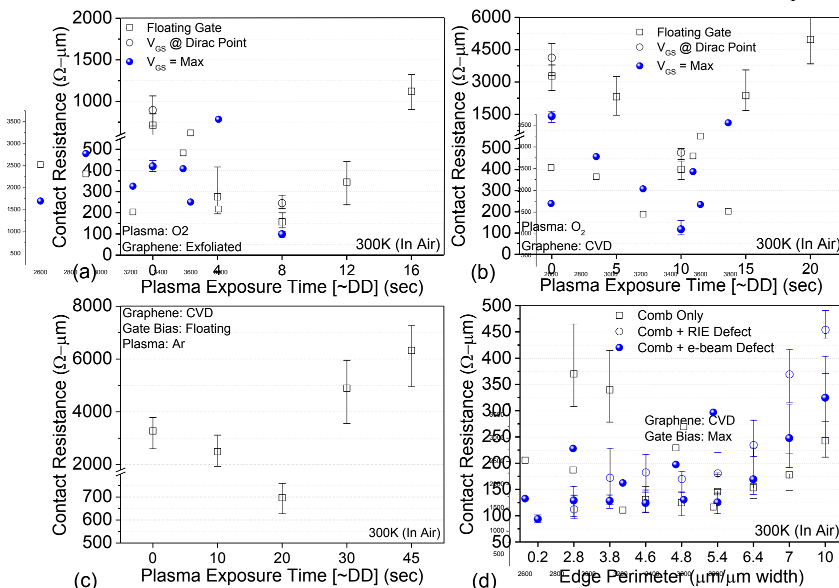


Fig. 7: Proposed methods to engineer the contacts to introduce additional sp – hybridized sites, as depicted in Fig. 5a. (a) An O$_2$/Ar plasma or O2/Ar ion bombardment is used to introduce defects. O$_2$ plasma leads to chemical removal of carbon atoms, whereas other methods lead to physical removal. (b) A highly energetic electron beam was used to locally burn graphene region. Here electron beam was scanned through the contact area, before depositing metal, with finite x – y steps. In case of O$_2$/Ar plasma, RF power was optimized to a very low value and then time for which devices were exposed to plasma was varied. An increased exposure time is expected to increase defect density (DD) or sp–hybridized sites.



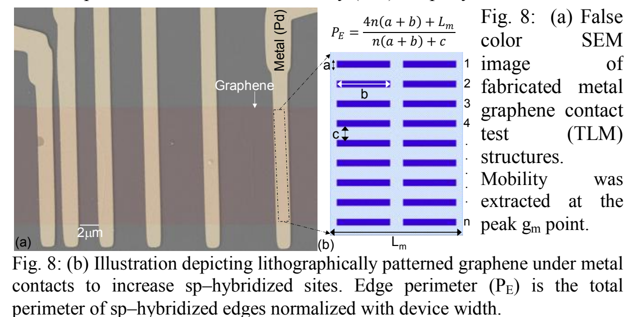


Fig. 8: (a) False color SEM image of fabricated metal graphene contact test (TLM) structures. Mobility was extracted at the peak g_m point.

Fig. 8: (b) Illustration depicting lithographically patterned graphene under metal contacts to increase sp–hybridized sites. Edge perimeter (P_E) is the total perimeter of sp–hybridized edges normalized with device width.

Fig. 9: Contact resistance extracted using fabricated TLM test structures as a function of (a) O$_2$ plasma exposure time for exfoliated graphene, (b) O$_2$ plasma exposure time for in-house grown CVD graphene, (c) Ar plasma exposure time for in-house grown CVD graphene and (d) edge perimeter of lithographically patterned edges with O$_2$ plasma or electron – beam exposure. Here perimeter = 0.2 is the device with no comb geometry. For statistics, a minimum of 15 devices per exposure time or process type were tested. In total, the data presented in this figure is extracted from over 500 devices across 20 chips. Devices with 8 sec O$_2$ plasma exposure offer a least contact resistance of 78 Ω–µm (exfoliated), whereas the same using *ebeam* is 84 Ω–µm (CVD).

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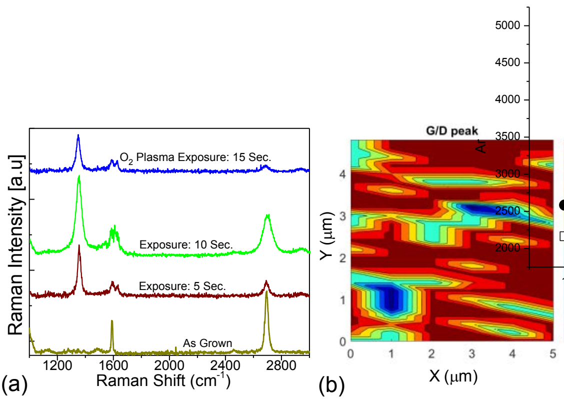


Fig. 10: (a) Raman spectrum extracted for as grown graphene monolayer as well as graphene exposed to O_2 plasma with different exposure times. (b) G/D peak extracted across 5µm × 5µm of graphene area exposed to O_2 plasma for 10 seconds.

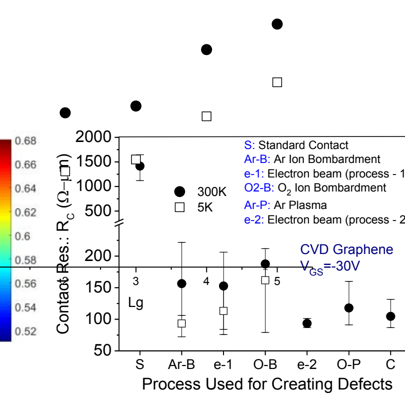


Fig. 11: Metal – graphene contact resistance of standard vs. engineered contacts while using various different techniques proposed above. The least contact resistance by Ar ion bombardment is 94 Ω–µm (CVD graphene) and by electron beam (process 1) is 84 Ω–µm (CVD graphene), at room temperature.

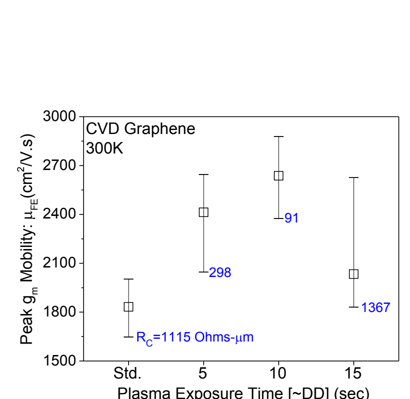


Fig. 12: Impact of plasma exposure time on contact resistance and it's correlation with channel mobility. Channel / field effect mobility is extracted at peak g_m.

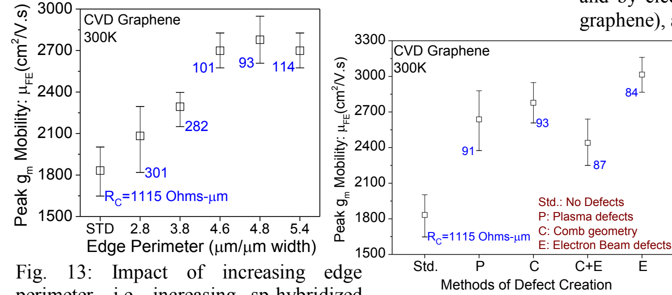


Fig. 13: Impact of increasing edge perimeter, i.e. increasing sp-hybridized sites on contact resistance and its correlation with channel mobility. A significant improvement in mobility can be observed by increasing the sp – hybridized carbon sites.

Fig. 14: Method of defect creation, least resistance achieved and its impact on channel mobility.

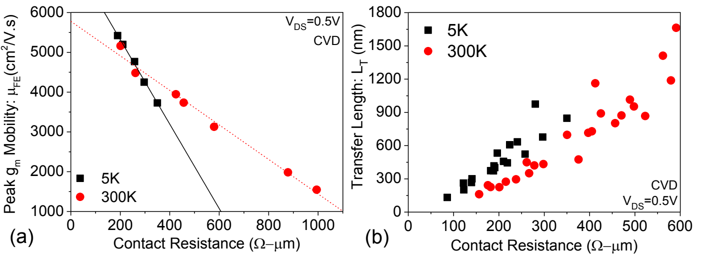
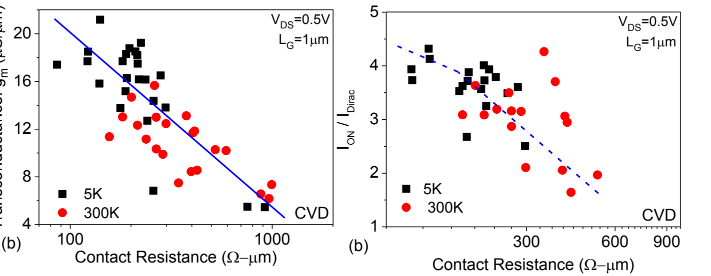


Fig. 15: (a) Channel mobility and (b) transfer length as a function of contact resistance, extracted at 5K and 300K. Figure shows that mobility increases by >5× and transfer length scales below 150nm when contact resistance was lowered down to 80 – 100 Ω–µm.

Fig. 16: (a) ON current (I_{ON}), (b) transconductance and (c) I_{ON}/I_{Dirac} as a function of contact resistance, extracted at 5K and 300K. I_{Dirac} is current measured at the Dirac point. Figure shows that device figure of merit parameters like I_{ON}, gm and I_{ON}/I_{Dirac} improves significantly when contact resistance was scaled below 100 Ω–µm.



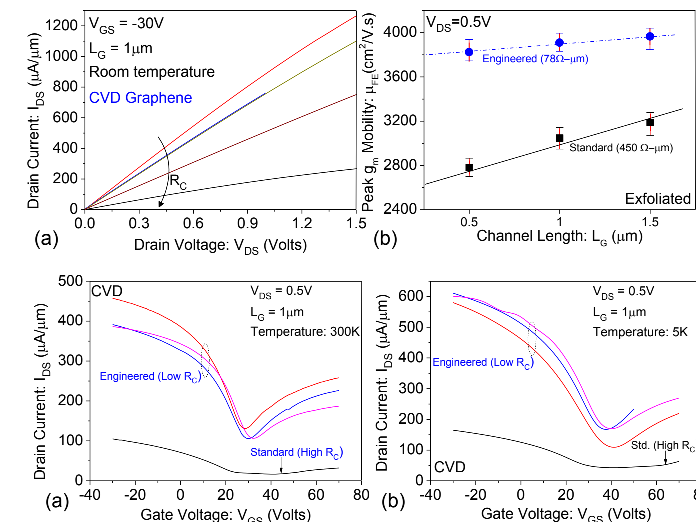


Fig. 17: (a) I_{DS} – V_{DS} characteristics as a function of contact resistance, (b) channel mobility vs. channel length for engineered vs. standard contact and (c) Transistor scaling characteristics for engineered contact devices depicting I_{ON} improvement (∝1/L) as channel length was scaled. Scaling behavior was not evident in standard devices attributed to reduction in mobility and contact limited current at shorter channel lengths.

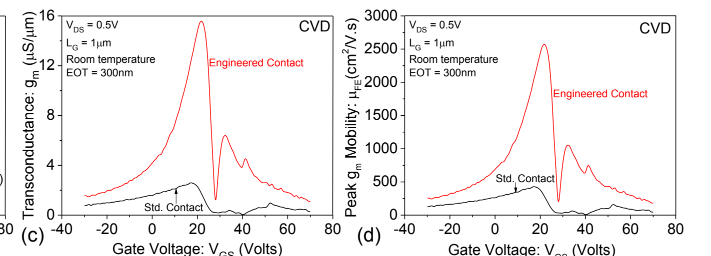


Fig. 18: (a) – (b) I_{DS} – V_{GS} characteristics of back-gated graphene FETs with and without engineered contacts measured at 5K and 300K, respectively. (c) Transconductance and (d) channel field effect mobility as a function of applied back gate bias, for devices with and without engineered contacts.

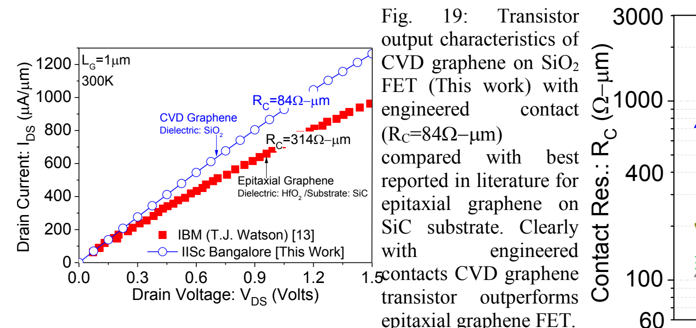


Fig. 19: Transistor output characteristics of CVD graphene on SiO_2 FET (This work) with engineered contact (R_C=84Ω–µm) compared with best reported in literature for epitaxial graphene on SiC substrate. Clearly with engineered contacts CVD graphene transistor outperforms epitaxial graphene FET.

Fig. 20: Graphene – metal contact resistance reported till date by various groups compared with contact resistance reported in this work for both CVD and exfoliated graphene. We show 138% and 28% lower contact resistance when compared to best reported till date for CVD and epitaxial graphene, respectively.

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