On the Design Challenges of Drain Extended FinFETs for Advance SoC Integration

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***Abstract*—In this paper, for the first time, challenges associated with high voltage drain extended device design in nanoscale FinFET technology is discussed in context of System on Chip (SoC) integration. Using 3D technology CAD, performance figures of merit matrix for integrated switching applications, quasi saturation, device scaling, ESD reliability, self-heating behavior and Safe Operating Area (SOA) concerns are comprehensively correlated/compared with planar drain extended MOS device.**

Keywords— Drain extended FinFET; DeMOS; ESD; Quasi-Saturation; SOA

I. INTRODUCTION

Planar bulk MOSFETs have reached its scaling limits and the evolution of FinFET technology has dragged much attention in the recent times. FinFETs are serving as a substantial replacement for bulk MOSFET for sub-20nm technology [1] [2]. Design, economy and cost to performance always remains as a challenge [3]-[5]. Besides this Process design co-optimization was driven for SoC development [6],[7]. Despite of the advancement in the FinFET technology, not much leap has taken forward on the high voltage (HV) tier, due to the fragility imposed by lean fins as wells as the reliability and heating aspects driven by the high current densities. Improvement of the on resistance R_{ON} and Breakdown voltage V_{BD} trade off was demonstrated in HV-FinFET [8]. However, a detail study to opt for all fin's design for SoC applications was missing in the literature. The following sections of the manuscript summarizes the challenges/de-merits associated with the conventional designing of Drain extended FinFETs (DeFinFET), and concludes with the necessity of newer device designs for realizing HV FinFETs.

II. DEFINFET : DEVICE DESIGN

A 3D view of TCAD simulated conventional DefinFET architecture is shown in Fig. 1(a) and an associated schematic is shown in Fig. 1(b)-(c). TiN is used as a gate metal, HfO2 and SiO2 as gate oxide with an Effective Oxide Thickness (EOT) of 1.1nm. Here the N/P triple well and low doping concentrated N-Well with a gate overlap on N-Well as a field plate is employed for effective Reduced Surface Electric Field (RESURF). And a body is contacted for the P-Well which is separated by a Shallow Trench Isolation (STI). Keeping the technology parameters intact, the architecture of the DeFinFET is extended with a well calibrated FinFET setup as shown in Fig. 2 [9]. The planar counterpart of the DeFinFET, i.e., DeMOS is engaged for the performance and Figure of merit explorations All the simulation work is carried out by Sentaurus TCAD suite[10]

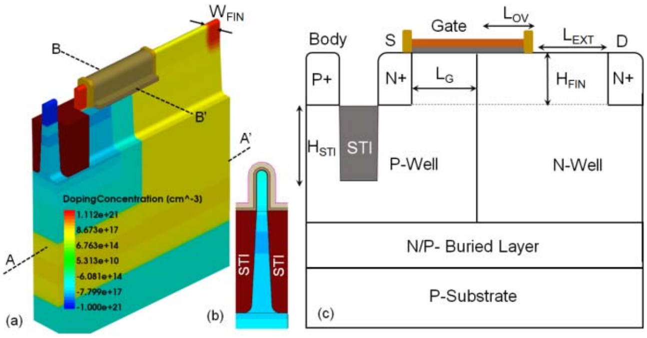

Figure 1: (a) 3D view of the Drain extended FinFET (DeFinFET) used in this work. (b) Cross-sectional view of Fin region inside the channel, along cutline B-B' (c) cross-sectional view of the device under study, along the cut line A-A'. Negative buried layer using deep N-type well is shown here; however, design of experiments consists of P-type super junction layer as well in place of N-buried layer.

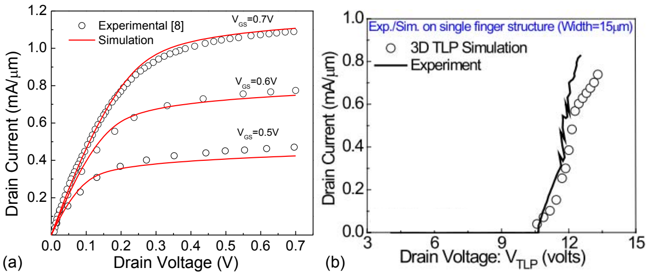

Figure 2: Calibration of mobility, avalanche (coupling with thermal boundaries) for FinFET device [9]. (a) Calibration of mobility including fin confinement effects MOS operation (b) Calibration of Avalanche and velocity saturation models with thermal boundaries for planar DeMOS for High current operation [11].

III. DEVICE PERFORMANCE AND DISCUSSION

Fig. 3(a) depicts the R_{ON} vs V_{BD} trade off comparison of planar and fin enabled drain extended devices. Fig. 4 depicts the band diagram of DeMOS and DeFinFET, it is clear that

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unlike DeMOS, the unaltered slope of band diagram of fin under the gate, makes V_{BD} ineffective towards change in gate length (L_G) (Fig. 3(c)). However, V_{BD} gets sensitized towards drain extension (L_{EXT}) linearly as seen through Fig. 3(d). And is attributed to the steep band bending in L_{EXT}. Based on the band diagram estimation, channel length scaling in DeFinFET becomes easier, since the fin enablement controls the short channel effects.

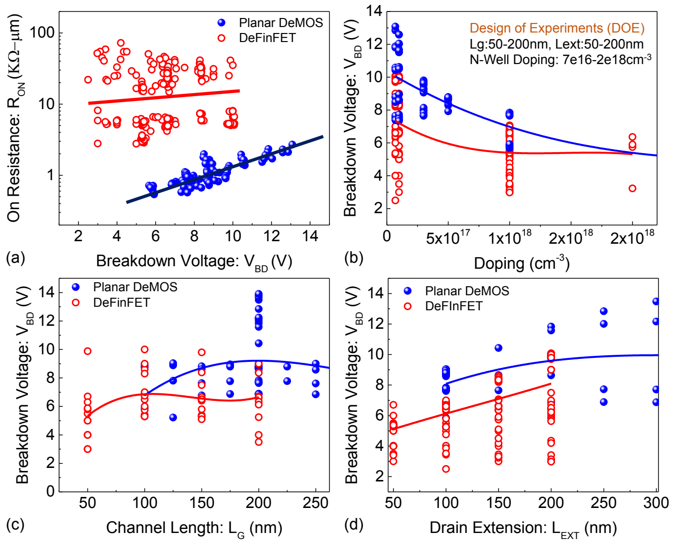

Figure 3: A comparison of simulated (a) ON resistance vs. breakdown voltage; (b) breakdown voltage vs. well doping; (c) breakdown voltage vs. channel Length and (d) breakdown voltage vs. drain extension length trade-offs for DeMOS and DeFinFET.

Therefore, DeFinFETs for a high V_{BD} target by large L_{EXT} appends large resistance due to its narrower fin. Moreover, the deeper wells do not recover the R_{ON} vs V_{BD} tradeoff as it does in the DeMOS. Due to fin geometry and wrapped gate over fin, does not leave much scope to control V_{BD} towards the P-well doping and spacing, like it can be controlled in its planar counterpart. Hence, from Fig. 3(a) it is seen that conventional device design for FinFET comes with ~10X increment in R_{ON}. However, the rate of ON resistance increment is more severe in planar DeMOS as compared to the DeFinFETs. Moreover, extended fin not just increases R_{ON}, but also leads to an early quasi saturation, when compared to planar DeMOS. Early Quasi-Saturation is attributed to an early space charge modulation (SCM) [12] in DeFinFET, attributed to narrow fins.

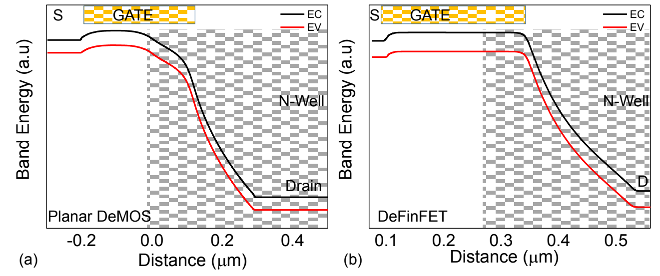

Figure 4: Energy band diagram of (a) Planar DeMOS and (b) DeFinFET, extracted near the channel region. Missing short channel effect (drain induced barrier lowering) and potential for channel length scaling is evident for DeFinFET.

Since the space charge modulation is a current density driven phenomena, fin procured high current density cause pronounced quasi saturation at an early gate bias. As depicted in Fig 5(a), when the current density exceeds background doping, a shift in the peak electric field is observed, which in turn degrades the carrier mobility in the extended region and limits the current flow due to field screening [13],[14]. As a result, drain current saturates as a function of gate voltage as shown in Fig. 5(b). Since the quasi saturation is primarily triggered due to the high current densities, DeFinFET's suffer the worst scenario of quasi saturation. As a result, Fig. 6(a) shows the severe reduction in the ON current for a same operating voltage class. However, the rate of decrement in ON current over the change in V_{BD}, is much severe in case of planar DeMOS, and has ~8X times higher rate of decrement in the I_{ON} when compared to DeFinFETs.

However, due to the advantage of fin geometry, Fig. 6(b) shows significant reduction in the leakage current when compared to its planar counterpart. Fig. 7(a) shows the Figure of Merit (FOM) comparison of planar and FinFET drain extended devices. Quasi saturation/ Fin-geometry imposed current and R_{ON} degradation makes DeFinFETs inferior towards planar DeMOS in terms of FOM. Fig. 7(b) on the other hand, in the pre quasi-saturation regime of the transistor operation, i.e., the gate bias at peak g_m, DeFinFETs offers less self-heating as compared to its planar counterpart.

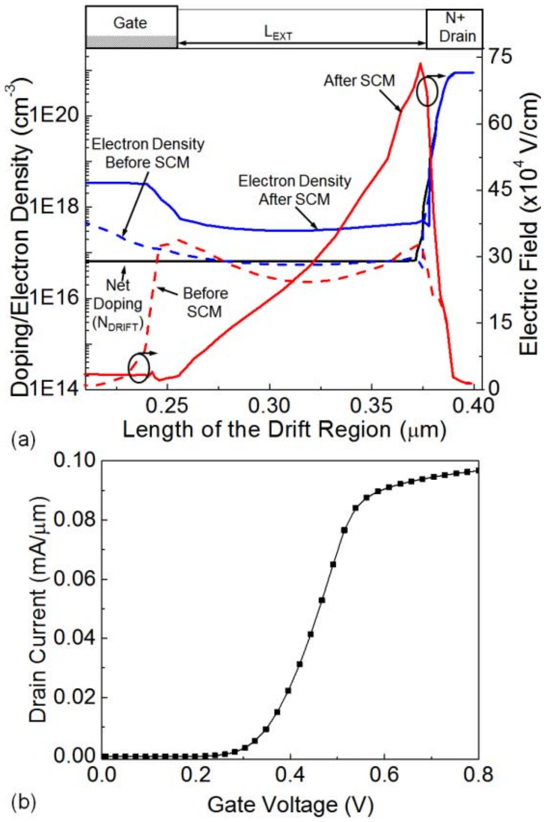

Figure 5: (a) Representation of space charge modulation in DeFinFET, Electric field (red), electron density (blue), (b) Transfer I-V characteristics with quasi-saturation.

IV. SELF-HEATING AND SAFE OPERATING AREA

Self-heating/hot spot of the drain extended devices at high current injections is mostly localized at the N-/N+ drain junction. This is attributed to the localization of the electric field caused by SCM. Moreover, it is worth highlighting from Fig. 8, that DeFinFET unit cell shows a hot spot formation whereas, the planar DeMOS shows a localized filament across the width of the device. Filament formation in the devices leads to a catastrophic failure and causes meltdown. However, absence of filaments in DeFinFETs multi-finger configuration makes the device more attractive for SoC integration.

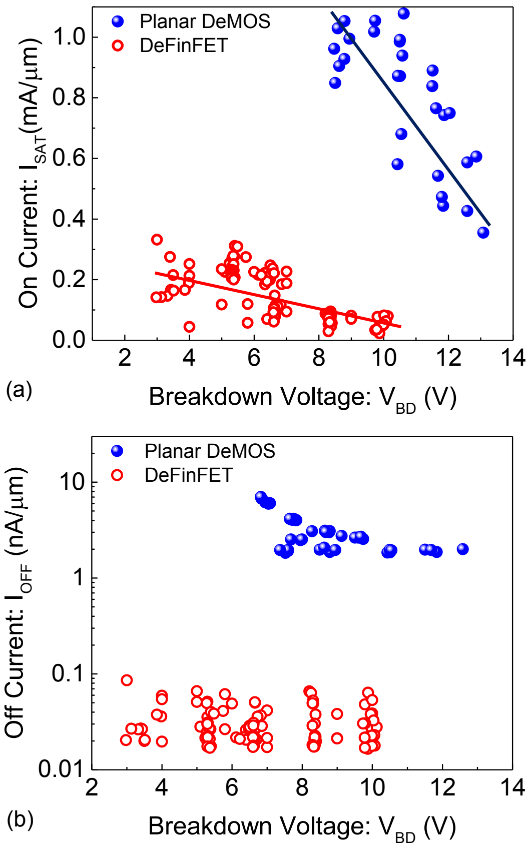

Figure 6: A comparison of (a) ON current, and (b) OFF current of planar DeMOS and DeFinFET extracted from a DOE.

Due to the filament driven high current crowding in planar DeMOS, DeFinFET in Fig. 8(a) offers an extended/Large SOA (when extracted using transmission line pulsing (TLP) method). Moreover, in Fig. 8(b) up to 4 finger configured DeFinFET's does not show any deterioration. Unlike planar DeMOS, after space charge modulation where the current is pulled closer to evolve into a filament under the TLP stress, DeFinFET compartmentalize current, subjugated to the fin geometry/ Fin isolation. Due to the nature of the discreet current flow in the form of fins, filament formation can be largely suppressed. However, filaments prediction in the large array of DeFinFETs still remains as a quest to probe further. To summarize, DeFinFETs can survive as a self-reliable device due to its robustness toward the TLP stress, when compared to its planar counterpart.

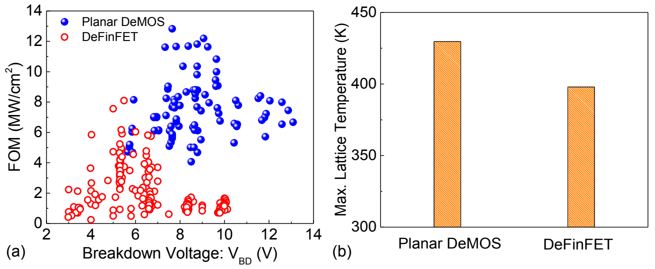

Figure 7: (a) Figure of Merit (FOM) $V_{BD}^2/R_{ON\text{-}sp}$ and, (b) Lattice Temperature comparison of planar and FinFET drain extended devices. For lattice temperature simulations, devices were biased at peak gm point while keeping drain voltage = $V_{BD}/2$.

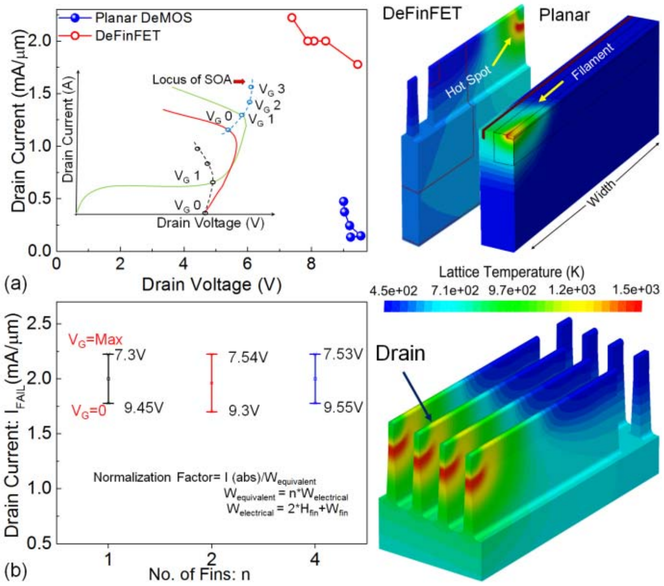

Figure 8: Safe Operating Area (SOA) boundary extracted for planar DeMOS and DeFinFET devices using 3D / multi-Fin electro-thermal simulations. Contour plots depict filament formation in DeMOS devices, which however is missing in DeFinFET.

V. CONCLUSION

Attributed to the narrow Fin geometry, devices were found to experience an early quasi-saturation, which seriously challenge the design of high voltage drain extended MOS devices in FinFET technology, when compared to its planar counterpart. However, on the other hand, due to improved channel control in Fin based geometry, DeFinFET's were found to allow channel length scalability, which is often missing in high voltage planar counterpart. In addition to this, rate of ON resistance vs Breakdown voltage trade-off observed to be less severe in DeFinFETs as compared to planar DeMOS. Moreover, due to distributed nature of fins in a multi-fin (large active width) DeFinFET device, non-uniform turn-on across Fins was missing under high current injection conditions. This resulted in an improved SOA boundary, unlike planar counterpart. On the contrary, planar DeMOS devices fail due to an early filament formation. Therefore, in terms of robustness towards heating, the choice of DeFinFET in a multi-finger configuration for SoC applications over the planar DeMOS can be predicted.

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