

# Dependence of Avalanche Breakdown on Surface & Buffer Traps in AlGaIn/GaN HEMTs

Vipin Joshi\*<sup>†</sup>, Bhawani Shankar\*, Shree Prakash Tiwari<sup>†</sup> and Mayank Shrivastava\*  
 \* Advanced Nanoelectronic Device and Circuit Research Laboratory, Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore, Karnataka 560012, India; <sup>†</sup>Department of Electrical Engineering, Indian Institute of Technology Jodhpur, Jodhpur, Rajasthan 342011, India  
 email: mayank@dese.iisc.ernet.in

**Abstract**—For the very first time, influence of traps on avalanche breakdown of AlGaIn/GaN HEMTs is discussed. Impact of surface and bulk traps on breakdown voltage and device scaling is discussed with associated physics. Surface trap's were found to cause distinct breakdown characteristics with breakdown point varying from gate edge to drain edge, depending on nature, type and concentration. Buffer traps too influence the electric field near gate edge and leakage through the device, thereby affecting breakdown voltage accordingly.

## I. INTRODUCTION

AlGaIn/GaN HEMTs are one of the most promising candidates for high power and RF applications. However, due to their growth conditions, defect/dislocation generated bulk traps and surface traps are common in these devices [1]. Effect of these traps on device's DC and RF performance parameters is well explored [2]–[4], however, its impact on breakdown behavior of the device is not well understood. Recently, Shankar et al. [5] highlighted role of traps on Safe Operating Area (SOA) and avalanche behavior of these devices. Figure 1, shows that under UV illumination SOA of the device improves as compared to that under dark conditions [5], suggesting that traps might be limiting SOA of the device. Also, negligible degradation in the DC current of the device under stress with UV exposure (Fig. 2b) suggests trap related degradation under dark conditions (Fig. 2a) [5]. These characteristics of the device under UV and dark conditions clearly outline how traps can limit breakdown performance of the device. Since surface states modeled as donor type traps and bulk traps modeled as acceptor type traps affect the 2-Dimensional Electron Gas (2-DEG) charge density, they will have a significant impact

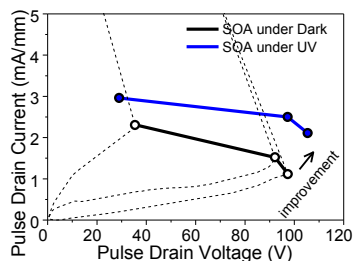


Fig. 1. IV characteristics with Safe Operating Area for an AlGaIn/GaN HEMT. Significant improvement in SOA boundary with carrier detrapping (UV) can be observed [5].

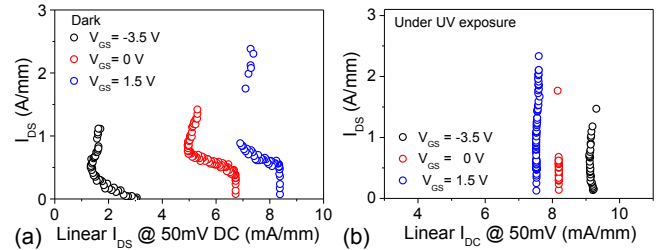


Fig. 2. (a) Linear drain-to-source ( $I_{DS}$ ) current degradation is measured after each voltage pulse, under dark condition. (b) Measurements under UV (365 nm) exposure result in negligible degradation in  $I_{DS}$ . Presence of UV light enhances carrier emission from surface and bulk traps and mitigates device degradation [5].

on depleting the channel and hence will also affect electric field in the region. This work for the first time establishes the effect of traps on device's breakdown performance in terms of scaling and also establishes the physics behind it.

## II. SIMULATION SETUP

Simulation setup used in this study is based on the modelling approach as defined in our earlier work [2], with an addition of impact ionization model according to the Chynoweth law [6] with critical field values set for GaN at  $3 \times 10^6$  V/cm. In this work, the device under study is an AlGaIn/GaN HEMT with source connected field plate structure [7], as shown in Fig. 3a. Figure 3b compares the experimental results [7] with simulated results. The figure clearly indicates a good agreement between the simulated and experimental data.

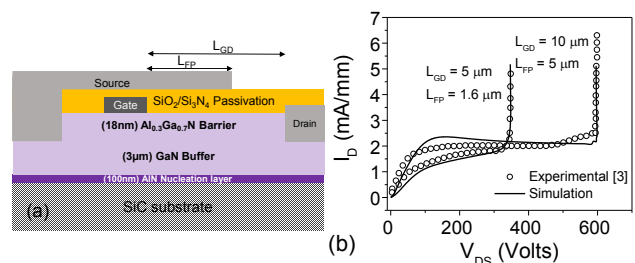


Fig. 3. (a) Cross-sectional view of AlGaIn/GaN HEMT layer stack [3] used in this study. (b) Comparison between experimental[3] and simulated data for the AlGaIn/GaN HEMT device.

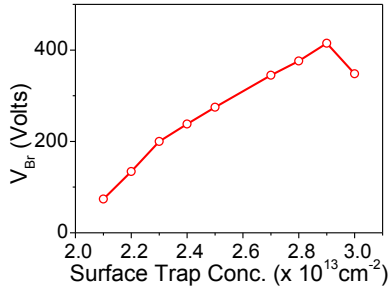


Fig. 4. Initially breakdown improves with surface trap concentration but later on decreases with shift in breakdown point from drain edge to gate edge.

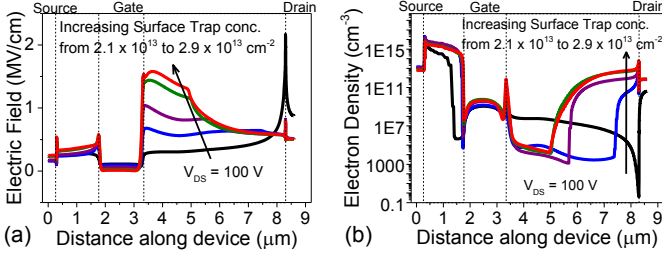


Fig. 5. (a) Electric field and (b) Electron density in the channel region as a function of surface trap concentration. With increase in surface trap concentration the field starts peaking towards gate edge, effectively redistributing in the whole channel region.

### III. SURFACE STATES/TRAPS

Surface states are prominently known as the source of charge for the 2-DEG channel [8]. Also several effects like DC-RF dispersion, gate and drain lag, etc. and their mitigation with use of a passivation layer, suggest these surface states to behave as traps. These traps have to be effectively donor in nature in order for a 2-DEG channel to exist [8]. In this work, surface states are modeled as donor type traps with an energy of 0.6 eV relative to the conduction band energy of AlGaIn. This particular energy of  $E_C - 0.6$  eV is associated to surface traps in AlGaIn layer [1]. Figure 4 suggests that the breakdown voltage initially increases with surface trap concentration, which however falls later. This can be explained by examining electric field in the channel region and associated electron density as a function of surface trap concentration as shown in Fig. 5a and Fig. 5b respectively.

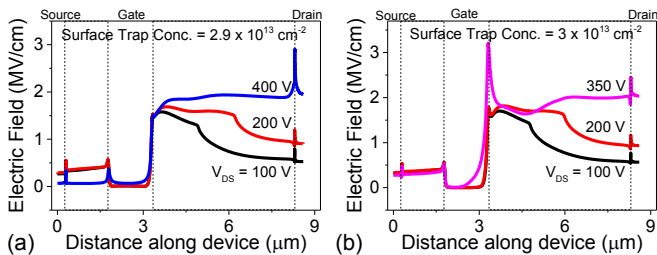


Fig. 6. Electric field profile in the channel region for surface trap concentration of (a)  $2.9 \times 10^{13} \text{ cm}^{-2}$  and (b)  $3 \times 10^{13} \text{ cm}^{-2}$  at different drain bias voltages.

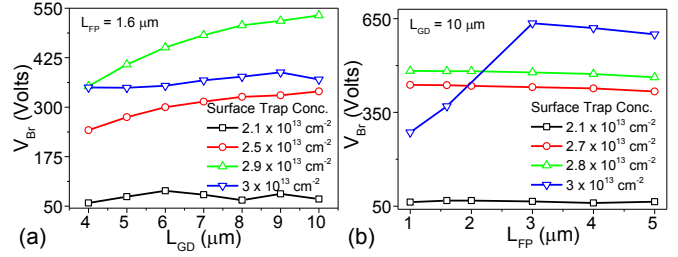


Fig. 7. Effect of (a)  $L_{GD}$  and (b)  $L_{FP}$  scaling on breakdown voltage as a function of surface trap concentration.

Surface traps being donor in nature provide charge carriers to the channel. Hence for lower surface trap concentration, the channel charge density is lower and the depletion region extends rapidly to the drain edge (Fig. 5b), where the electric field peak can be observed (Fig. 5a). In case of higher trap concentration, due to surface traps behaving as charge suppliers, depletion region is confined near the gate edge and slowly extends towards drain electrode (Fig. 5b). This results in an effective redistribution of electric field in complete channel (Fig. 5a) for higher trap concentrations. Although the field initially increases near gate electrode, the breakdown finally happens near the drain electrode (Fig. 6a), due to extension of depletion region upto the drain electrode. On further increasing trap concentration the depletion region near gate electrode is narrow enough to cause sufficiently high electric field for breakdown (Fig. 6b). Further increasing trap concentration leads to higher gate leakage resulting in early breakdown of the device. Thus the breakdown region shifts from drain edge to gate edge with an increase in surface trap concentration.

### IV. EFFECT OF SURFACE TRAPS ON DEVICE SCALING

The physical design parameters to be considered for breakdown voltage improvement in AlGaIn/GaN HEMTs are gate to drain distance ( $L_{GD}$ ) and field plate length ( $L_{FP}$ ) as indicated in Fig. 3a. Figure 7a suggests that breakdown voltage does not scale with  $L_{GD}$  for very small trap concentrations. While it shows good scaling for higher trap concentration, but again scales at a low rate when trap concentration further increases. This can be explained by the electric field profile as shown in Fig. 5 and Fig. 6. For lower trap concentrations since the channel is completely depleted, the field peaks near the drain edge (Fig. 5a) and hence there is no scaling with  $L_{GD}$ . However, with increasing concentration as the field redistributes uniformly in the channel region (Fig. 6a), the breakdown voltage also scales with  $L_{GD}$ . However, at even higher trap concentrations, the depletion region does not expand and the field peaks abruptly near gate edge (Fig. 6b) and scales lesser with  $L_{GD}$ .

Breakdown voltage scaling for a device with constant  $L_{GD}$  and variable field plate length is shown in Fig. 7b. The figure interestingly shows a different trend than that for  $L_{GD}$  scaling. The device shows a considerable scaling with  $L_{FP}$  for much higher surface trap concentrations and doesn't show any scaling for lower trap concentrations. This can be explained by

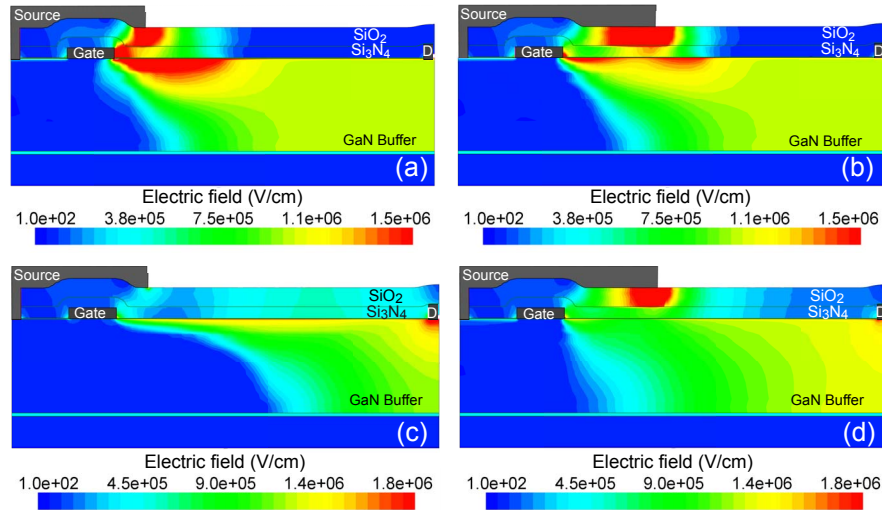


Fig. 8. (a) and (b) represent the effect of  $L_{FP}$  scaling in presence of a higher surface trap concentration of  $3 \times 10^{13} \text{ cm}^{-2}$ .  $L_{FP}$  is  $1 \mu\text{m}$  in (a) and  $3 \mu\text{m}$  in (b). Relaxation of field near gate edge due to field plate can be observed. (c) and (d) represent same effect with a lower surface trap concentration of  $2.7 \times 10^{13} \text{ cm}^{-2}$ . In this case since the field effectively peaks at drain edge, no relaxation is observed with a source field plate.  $L_{GD}$  in all the cases is  $10 \mu\text{m}$ .

electric field contour plots of Fig. 8. For devices with higher trap concentration (Fig. 8a and 8b), the field peak is near gate edge and is relaxed efficiently by source-connected field plate and enables improvement in breakdown voltage. On the other hand, for lower trap concentration, as the field peaks near the drain edge, use of a source-connected field plate is not able to relax this field (Fig. 8c and 8d). Thus the device doesn't show any improvement in breakdown voltage with increasing  $L_{FP}$ .

## V. BUFFER TRAPS

Traps in the GaN buffer are present due to dislocations/defects incorporated during the growth process. Since the unintentional doping in GaN buffer is known to be n-type in nature, these buffer traps have to be dominantly acceptor type in nature for the buffer to be semi-insulating and for a confined 2-DEG channel to be formed [9]. These dislocations/defects are modeled in this work as acceptor type traps with an activation energy of  $E_C - 0.96 \text{ eV}$  in GaN buffer. This energy level is suggested to be present in bulk-GaN due to dislocations [1]. Fig.9a shows the effect of buffer trap concentration on breakdown voltage of the device for different surface trap concentrations. For lower surface trap

concentrations, the breakdown voltage falls as the buffer trap concentration is increased. For higher surface trap concentrations, the breakdown voltage initially increases, reaches a peak and then again starts decreasing as the buffer trap concentration is further increased. This initial improvement can be explained by the electric field profile in the channel region for the two cases, as is shown in Fig. 9b. It shows that higher concentration of buffer traps relaxes electric field near the gate electrode and hence causes an improvement in the breakdown voltage. However, reduction in breakdown voltage with further increase in buffer trap concentration can be explained with contour plots of Fig. 10.

From current density contours, as shown in Fig. 10, it can be observed that as the buffer trap concentration is increased, initially the breakdown occurs near the gate edge and major current flows through gate electrode (Fig. 10a). With a further increase in trap concentration, Fig. 10b, leakage through buffer increases, however, still breakdown occurs near the gate edge and majority of current flows through gate. On further increasing the buffer trap concentration, a hole leakage path is formed through the parasitic hole channel on the GaN/AlN interface which is present due to polarization effect [2]. Since acceptor type buffer traps assist this hole current to flow, any further increase in trap concentration causes the breakdown voltage to reduce (Fig. 9a). SEM images for an AlGaIn/GaN HEMT, as shown in Fig. 11 and 12, for device failure under UV and dark conditions are in good agreement with this observation. It can be seen that in dark condition, cracks are formed in the Gate-Source region, simulations also suggest that under high buffer trap concentration leakage between Gate-Source starts increasing (Fig. 10c). Also, under UV conditions (Fig. 12), which can be considered as low trap concentration case, cracks are formed under gate and propagate towards drain, which is similar to simulated case of Fig. 10a.

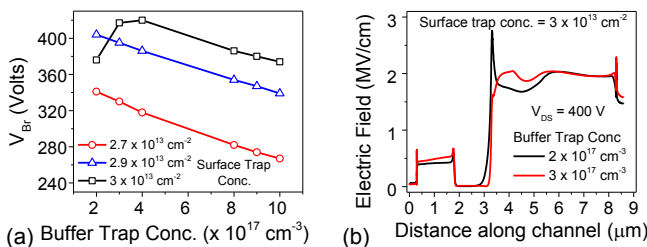


Fig. 9. (a) Breakdown voltage as a function of acceptor type buffer traps. (b) Electric field relaxation near gate edge can be observed with higher buffer trap concentration, for a surface trap concentration of  $3 \times 10^{13} \text{ cm}^{-2}$ .

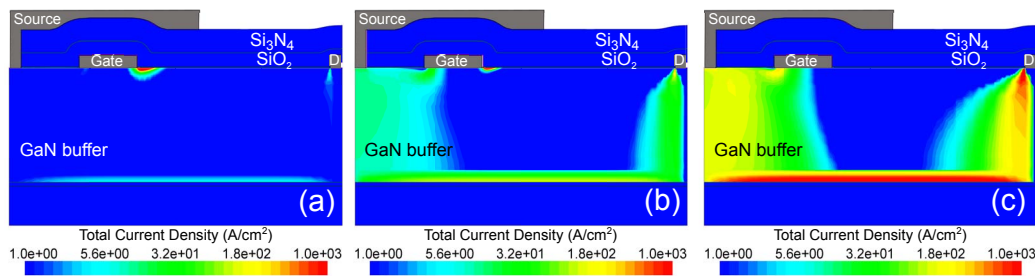


Fig. 10. Contour plot of total current density for buffer trap density of (a)  $2 \times 10^{17} \text{ cm}^{-3}$ , (b)  $3 \times 10^{17} \text{ cm}^{-3}$  and (c)  $1 \times 10^{18} \text{ cm}^{-3}$ .

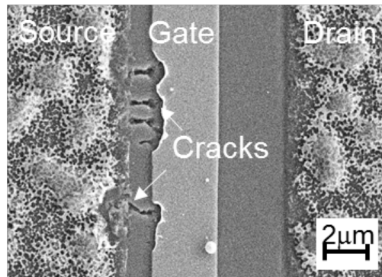


Fig. 11. Post failure SEM micrograph of the device tested under dark. The figure highlights device failure occurs in gate-source region under dark condition which is similar to observations for higher buffer trap condition [5].

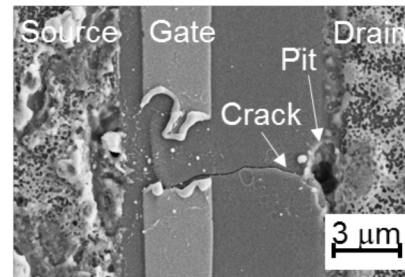


Fig. 12. Post failure SEM micrograph of the device tested under UV. With UV exposure failure occurs predominantly in gate-drain region as seen for lower buffer trap condition [5].

## VI. CONCLUSION

The physics behind experimental evidence of dependence of avalanche breakdown on surface & buffer traps in AlGaIn/GaN HEMTs was discussed for the first time. Increase in surface trap concentration modifies the depletion region, resulting in a shift in failure point from drain to gate edge. While devices with lower surface trap concentration didn't show any scaling of breakdown voltage with device's physical dimensions, moderate surface trap concentration devices showed a considerable scaling with  $L_{GD}$ . A large surface trap concentration resulted in a weaker scaling with  $L_{GD}$ , owing to confined depletion region near gate edge. However, the trend was not similar for variations in field plate length and only devices with breakdown near gate edge showed a considerable improvement with field plate length scaling. This was only possible at sufficiently high surface trap concentrations. Buffer traps were found to influence electric field near gate edge in cases with sufficiently high surface trap concentration to result in an electric field peak near gate edge. In all other cases, buffer traps were found to degrade breakdown performance of the device. This was attributed to acceptor nature of these traps, which in turn assists leakage through parasitic hole channel at the buffer/nucleation layer interface. Further, the variations observed with buffer trap concentration were found to be in excellent agreement with SEM failure analysis of the device.

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