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Performance and Reliability Insights of Drain Extended FinFET Devices for High Voltage SoC Applications

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***Abstract*—In this paper[1], Drain extended FinFET device design and the challenges associated with the performance and reliability are discussed. Physical insights into the performance vs. reliability trade-off for the Fin enabled high voltage designs is elaborated and compared with their planar counterpart (DeMOS). Effect of Fin width discretization over ESD reliability, Safe Operating Area and HCI reliability are discussed.**

Keywords—Drain Extended, , ESD , finFET, HCI, reliability, Safe Operating Area

I. INTRODUCTION

Drain Extended MOS (DeMOS) devices were extensively implemented for high voltage (HV), System on Chip (SOC) applications [1]. Wide voltage range of LDMOS devices are used as gate drivers, voltage converters and operational amplifiers. On the other hand, with the aggressive CMOS scaling and with the advent of FinFET technology [2], the novelty of FinFETs served extensively in IC technology beyond 20nm. However, HV integration such as drain extended device technology did not pace up substantially for FinFET technology. Stacking the core/IO transistors can also offer high voltage applications for FinFET, but they are not only limited to few volts of operation and but also adds complexity of design, such as isolation schemes. One step solution for high voltage applications are DeFinFET devices. Where the operating voltage can be tuned with layout and other design parameters. Moreover, thermal resistance, power density, off state dissipation [3][4] threatens the feasibility of the FinFET HV integration. Performance metrics of fin-based HV devices [5]-[7] were discussed so far. However, detailed analysis of performance and reliability were never explored for fin enabled drain extended devices. This work demonstrates the performance and unique features of reliability of drain extended FinFET devices compared to its planar counterpart.

II. DRAIN EXTENDED FINFET: ARCHITECTURE AND DEVICE DESIGN

Fig. 1 shows the various cross sections of drain extended FinFETs. Proposed process FEOL flow for realizing the high voltage DeFinFET into the fin based technology is designed using 3D TCAD process simulations. Deep Wells for Drift region is implanted and annealed prior to baseline FinFET Process. In FinFET technology since the anneal cycles are shorter to control the depth of implants, high voltage wells suitable for DeFinFETs are implanted prior to the standard process flow the FinFET technology. Gate oxide used is a composure of SiO2 and HfO2 with Effective oxide thickness of 1.1nm, TiN is used as a gate metal and nitride spacers are used for contact isolation. The drain extended part of the device is formed with low doped drift region, unlike having a self-aligned source/drain contact, a selective source/drain contact formation is necessary. Fig. 2 shows the calibrated IV characteristics of FinFET with experimental data [8]. Device simulations and physical investigations are done using the FinFET calibrated setup.

A. On Resistance vs. Breakdown trade-off

Fig.3 shows R_{ON} vs V_{BD} tradeoff of HV-FinFETs ((a)DeFinFET and (b)STI-DeFinFET) in comparison with its

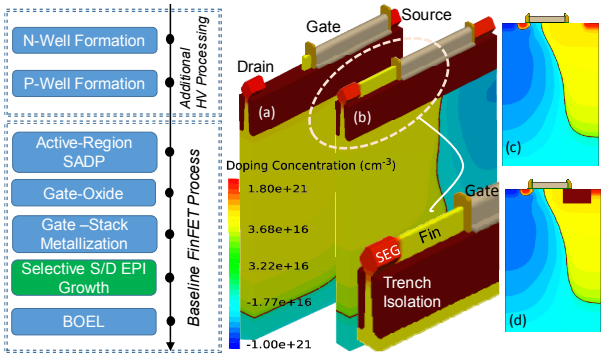

Figure 1: Proposed process FEOL of HV Drain extended devices, (a) STI-DeFinFET: STI isolation in the drift region (b) Drain extended FET: DeFinFET. Inset shows the Fin, Trench Isolation and Gate Metal Stack. (c), (d) are the planar counterpart DeMOS & STI-DeMOS respectively, which resembles the cross section of 3D-DeFinFETs.

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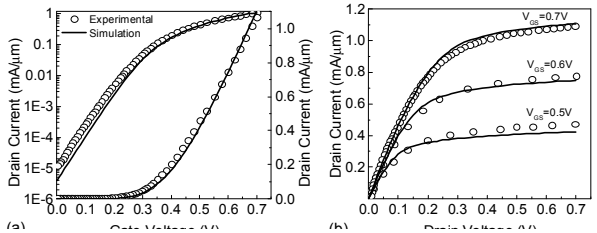

Figure 2: Calibration of TCAD models for drift-diffusion transport with experimental data [7] (a) Transfer characteristics, and (b) Output characteristics [6].

planar counterparts. HV-FinFETs with its architectural limitation of narrow width, shows higher R_{ON} over conventional DeMOS devices. DeFinFETs has an order trade off in RON vs VBD, when compared to planar technology. The inset of Fig. 3 shows the Design of experiments (DOE) used to tune the performance and voltage rating of the device. With the optimized design for RON vs VBD trade off, device with best performance out of DOE is chosen for reliability analysis of DeFinFET in the proceeding sections.

B. Quasi Saturation in DeFinFET

Fig. 4 depicts the quasi saturation behavior of DeFinFETs. With increase in gate bias and when high current is injected in to the drift region, the carrier density exceeds the background doping and causes space charge modulation. Fig. 4 (a) shows the shift in the peak from gate edge towards the drain edge of the device as a result of space charge modulation [9]. Fig. 4(b) shows the current saturation as a function of gate bias. The voltage range between threshold voltage and the onset voltage of quasi-saturation narrows down in DeFinFET, this is attributed to the narrow fin widths. Unlike planar DeMOS device narrow fin width in DeFinFET increases the current crowding and leads to the early quasi saturation effect.

C. DeFinFET : Figure of Merits

Fig. 5(a) shows the I_{ON}/I_{OFF} ratio of HV-FinFETs. Owing to the narrow pitch and fin enabled dual side channel inversion HV-FinFETs are benefited with good gate control over the channel and has low OFF state leakage. However, STI-DeFinFET due to high ON resistance has 2x times lower I_{ON}/I_{OFF} ratio, when compared to DeFinFETs. Current

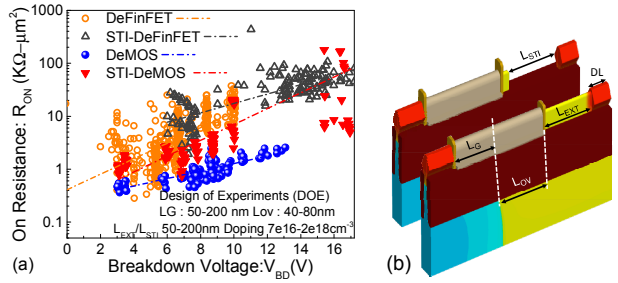

Figure 3: Performance Metric: (a) On Resistance (R_{ON}) vs Breakdown Voltage (V_{BD}) of DeFinFET and STI-DeFinFET devices. (b) 3D view of DeFinFET depicting channel length (L_G), Overlap Length (L_{OV}), Drift Length (L_{EXT}/L_{STI}) and drain contact length (DL).

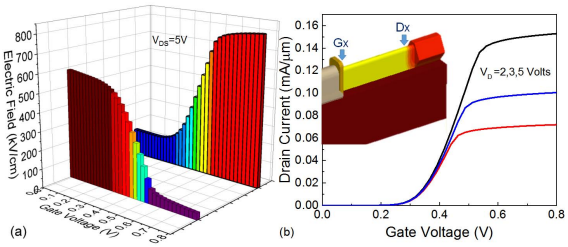

Figure. 4 (a) Quasi Saturation (QS) depicted through a shift in the peak electric field as a function of V_{GS},. Here Gx and Dx are referred to the position at Gate and Drain edge respectively as shown in the inset of (b), (b) transfer characteristics of DeFinFET depicting severe Quasi- Saturation at different Drain biases, is attributed to inevitable narrow fin architecture.

limitation phenomena of HV-FinFETs are described through quasi-onset current, Fig. 5(b) depicts the quasi onset current in DeFinFET and STI-DeFinFETs. Apart from having a narrow fin and device dimensions STI-DeFinFET is effected through severe quasi saturation. And this is attributed to higher current crowding under the drain contact opening. Moreover, space charge modulation is a current driven phenomenon, quasi saturation effect can be substantially lowered by increasing the drain opening (DL). Fig 5(b) inset shows the ~ 0.5x improvement in the quasi onset current.

Moreover, due to pronounced R_{ON} and current crowding in HV-FinFETs, Figure of Merit (FOM) stands 2x times lower (Fig. 6(a)) than Planar DeMOS and STI-DeMOS devices (Fig. 6(b)). The device foot print over the design of experiment of

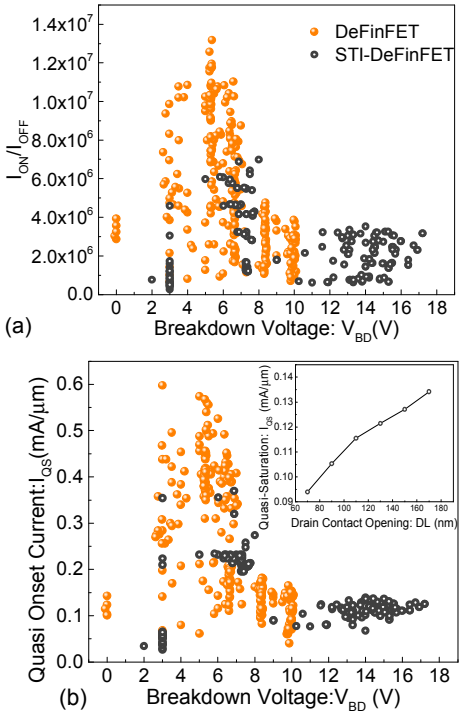

Figure. 5: (a) On Current I_{ON} to I_{OFF} ratio of DeFinFET and STI-DeFinFET devices(b) depicts the current at peak g_m (Quasi-onset) in I_{DS} vs V_{GS} characteristics. This is the current value at which kirk effect takes place. Inset shows the effect of drain opening (DL) on quasi onset current.

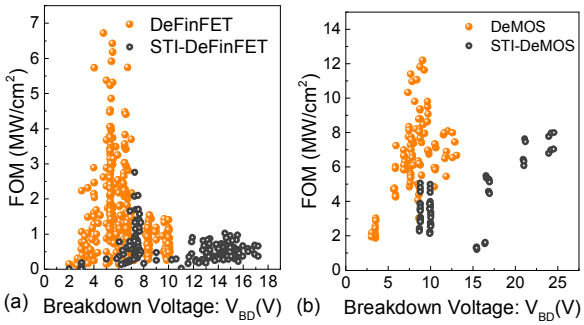

Figure. 6: Power rating of the transistor: Figure of Merit (FOM) of (a) DeFinFET and STI-DeFinFET measured as V_{BD}^2/R_{ON}-specific (b) FOM of Planar DeMOS in comparison with DeFinFET.

both the device types (planar and fin based) are identical. Inclusion of STI along the conducting path improves the V_{BD} by ~2X times by trading off with the FOM. However, Narrow pitch, wrapped gate and high current densities in HV-FinFETs severely degrades the performance when compared to its planar counterpart DeMOS devices

D. Band Tailoring in DeFinFETs

Fig. 7 shows the band diagram of DeFinFET taken under gate of Planar DeMOS whereas, the cutline for band diagram is taken inside the fin region of DeFinFET. Band bending extracted under the same biasing conditions, shows higher gradient being close to gate in Planar DeMOS while it is close to Drain contact in case of DeFinFET, this signature of band diagram reflects DIBL and hot carrier reliability favoring towards the DeFinFETs. Significant reduction of DIBL is seen in DeFinFET attributed to the pinning of band energy which comes from the wrapped gate around the fin. Since, the band bending is more towards the drain extension region in case of the DeFinFETs. Electric field is distributed more inside the drift region.

Due to this significant gate control over the channel is seen in DeFinFETs and owing to the band tailoring in the DeFinFET, the feasibility of channel length scaling is more flexible in fin based HV devices when compared to the planar DeMOS devices. Moreover, Drain induced barrier lowering also least effected in HV-FinFETs. Fig. 7(b) shows the effect of DIBL being more in case of Planar DeMOS when compared to DeFinFETs. Having compared the DIBL and

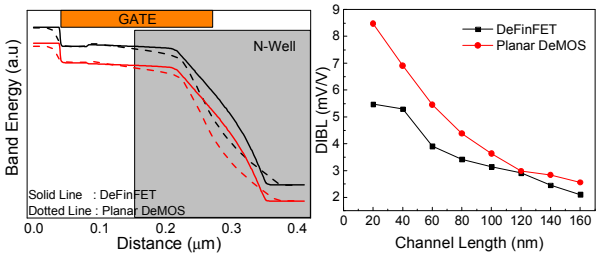

Figure.7: (a) Band Diagram comparison of planar DeMOS and DeFinFET, (b) Drain Induced Barrier Lowering (DIBL) comparison of planar DeMOS and DeFinFET. Significant reduction of DIBL is seen in DeFinFET attributed to the pinning of band energy which comes from the wrapped gate around the fin.

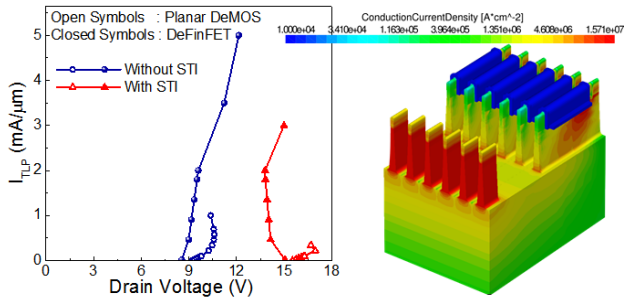

Figure. 8: (a) TLP IV characteristics of Planar DeMOS and DeFinFET (w/ and w/o STI). (b) Uniform current conduction during ESD stress in multifin configuration of DeFinFET.

channel control of DeFinFETs, ON current of fin based HV devices can be improved by scaling down the channel lengths. However, increasing the current in DeFinFET by channel length scaling will lead to the early quasi saturation effect. Therefore, DeFinFET performance gets trade-off between channel length scaling and ON current. Moreover, Quasi saturation in the device will lead to localized hot spot close to the drain edge, and increases the lattice heating and finally cause the device Failure.

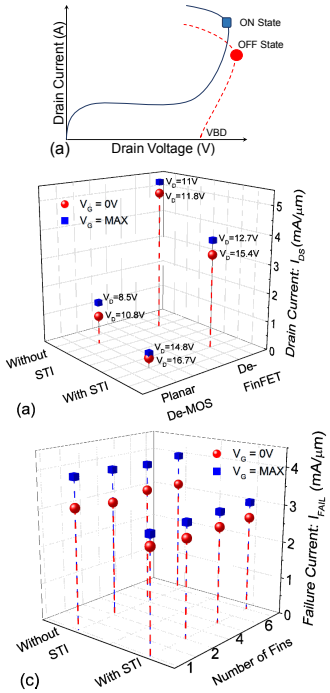

Figure. 9: Comparison of Safe operating area (SOA) of DeFinFETs and Planar DeMOS (a) SOA of drain extended devices are extracted using the failure current: It2. at ON state VGS =VGmax and OFF state VGS=0V. (b) Extraction method used to define SOA. SOA covered by the DeFinFETs is 5x times higher than its planar DeMOS counterpart. (c) SOA is independent of the multifinger arrangement in DeFinFETs, which makes them more suitable for HV integration over planar DeMOS devices

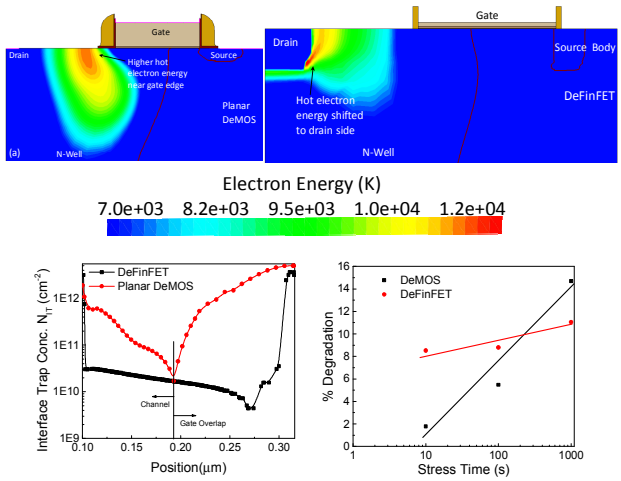

Figure. 10 Hot Carrier Induced (HCI) degradation Drain extended devices (a) Contour showing spatial hot carrier distribution in Planar and FinFET drain extended devices. In Fig. 7 Band bending signifies this phenomenal hot carrier distribution. Therefore, (b) NIT generation at oxide-silicon interface, shows, the degradation is concentrated at gate edge in DeFinFET, while NIT is distributed throughout the interface in Planar DeMOS(c) % Id-sat degradation of Planar and Fin DeMOS w.r.t time, where VDS is biased close to breakdown voltage. With the signature of NIT generation, the rate of degradation in Planar DeMOS is higher than DeFinFET.

III. RELIABILITY

Figure.8 (a) shows the ESD reliability Drain extended devices. Owing to filament formation, failure current It2 stands lower in planar DeMOS, whereas DeFinFET (w/ and w/o STI) can offer 5x times improvement in failure current. This is attributed to the isolation of the current path, coming from the fin to fin isolation. Contour plot in Fig. 8(b) shows the current conduction under TLP stress (a 100ns current pulse). Absence of current filamentation is shown through uniform current conduction. Fin enabled width discretization boosts ESD reliability. (Fig. 8(a)) and SOA (Fig. 9) of HV-FinFETs shows 5x times improvement in ESD reliability and 2x times improvement in SOA, which is attributed to mitigation of localized hotspots, which comes from uniform fin current (Fig. 9(b)), whereas planar devices show early failure signature due to formation of hot spots. Fig. 10 shows the HV-FinFETs having better tolerance towards HCI degradation, due to its nature of band bending. Hot carrier density distribution being away from the gate oxide region, favors in slower rate of degradation, whereas in Planar DeMOS Hot carriers are populated closer to gate edge leading to higher rate of degradation. Due to fin architecture, number of Si-H Bond Concentration will be greater than Planar architecture for a given device area/ foot print. Therefore, initial degradation, which is caused by Si-H bond breaking is significant in DeFinFET. However, the slope of degradation is higher in case of Planar DeMOS device, as the degradation of Si-O bond breaking is crucial over the overall stress period.

IV. SUMMARY

Fin based architecture and design for High voltage drain extended devices are studied. Attributed to narrow Fin geometry, quasi saturation onset appears early. Moreover, performance FOM of drain extended devices degrade severely as one moves for FinFET technology. However, on the other hand, due to fin enablement gate control over channel is improved. With the fin based architecture and observed band tailoring in DeFinFET are suitable for channel length scaling, where as in planar DeMOS, channel length scaling is often limited due to DIBL.Due to fin width discretization non-uniformity among the fins are suppressed in fin based High voltage devices. Fin width discretization favors in ESD reliability and SOA owing to uniform current conduction. And finally, since hot carrier density is distributed away from the channel region, the life time of the drain extended devices are predicted to increase in FinFET geometry.

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