Safe Operating Area (SOA) Reliability of Polarization Super Junction (PSJ) GaN FETs

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***Abstract*—For the first time, this work reports Safe Operating Area (SOA) assessment and degradation physics in Polarization Super Junction (PSJ) based GaN FETs made on Silicon and sapphire substrates under high voltage and high current injection conditions. Impact of device design parameters on SOA, associated trap assisted device degradation, and thermal failure are studied. Correlation between polarization super junction length and failure threshold is discovered, beside power and field dependence of SOA boundary.**

***Index Terms*—Polarization Super Junction, GaN FET, Safe Operating Area, Reliability.**

I. Introduction

Gallium Nitride has emerged as a promising semiconductor material because of its excellent properties like wide bandgap (3.4 eV), high breakdown field (3.3 MV/cm), low dielectric constant (9) and good thermal conductivity (1.3 W/cm-K). The Figures of Merit (FOM) calculations [1] clearly highlight the need for GaN based power devices to achieve higher frequency and high efficiency power electronics when compared to silicon devices, in a cost-effective manner. AlGaN/GaN HEMT owing to the existence of highly dense 2DEG (1×10^{13} cm^{-2}) with high electron peak velocity (2.5×10^{7} cm/s) and saturation velocity (1.5×10^{7} cm/s) has shown superior switching performance with better power efficiency than its Si counterparts, and there is an increasing thrust to further improve it. Polarization Super Junction (PSJ) concept, which is based on charge balance between high density 2DEG and 2DHG at the heterointerface, is recently introduced into the GaN FET family [2]- [6]. It can potentially overcome R_{ON} - V_{BD} trade-off in GaN HEMT by improving performance beyond its 1-D limit [2]. Recently, it is demonstrated that addition of PSJ to existing GaN MOS-HEMT improves its short circuit performance [7],[8]. Before, PSJ based GaN devices are deployed for widespread usage, it is crucial to understand the various degradation phenomena which can potentially limit their safe operation. The aim of this work is to investigate and evaluate the Safe Operating Area (SOA) reliability of PSJ based GaN FET under high voltage and high current injection conditions and understand the physics of failure/degradation, while considering the key design and technology parameters.

II. Device Architecture and Test Setup

This study uses, normally-ON PSJ based field effect transistors (FET) realized on Si and sapphire substrates. The devices use GaN/AlGaN/GaN material stack to realize super junction, as shown in Fig. 1. Source/drain contacts are based on commonly used Ti/Al/Ni/Au Ohmic stack and Ni/Au/p+ GaN based gate. Conventional HEMTs were also realized by selective etching of p-GaN and u-GaN layers on same wafer. Normally-ON transistors with different super-junction lengths (L_{PSJ}), with and without p-GaN/u-GaN in source-gate and gate-drain regions, were studied in this work. High voltage – high current characterization of devices was done using ultra-fast pulses of 100 ns duration with 1 ns rise time to determine the SOA boundary and failure threshold of devices. To monitor evolution of device degradation, linear drain to source dc current (I_{DC}) was spot measured at 50 mV after each stress pulse. Here, low dc bias is used to minimize device degradation if any during spot measurement. DC I-V and Capacitance-Voltage (C-V) characteristics of device were measured at regular intervals, during the test, to probe its degradation physics and failure mechanism. C-V characteristics were measured at low frequency (100 kHz) to capture maximum trap response. All the measurements were done at room temperature (300 K).

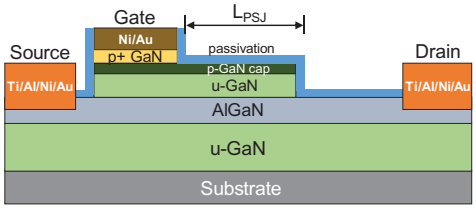

Figure 1. Cross sectional view of PSJ GaN FET with details of layer stack under-study. As depicted, SiO_2 passivation covers the channel consisting gate finger and acsess regions. Devices w/ & w/o u-GaN in the gate-drain region and with different super junction lengths (L_{PSJ}) were tested.

III. SOA Boundary And Power-To-Fail

Pulsed I-V characteristics were measured for PSJ-FET and conventional HEMT as shown in Fig. 2(a). PSJ-FET shows broader SOA boundary than compared with conventional HEMT. SOA boundary of a device is determined by the power sustained by it before the permanent failure. So, Power-to-Fail (P_{FAIL}) was measured in each case. Here, P_{FAIL} is a product of breakdown voltage (V_{BD}) and failure current (I_{FAIL}). Then P_{FAIL} was recorded for device with different super junction length (L_{PSJ}) and the result is plotted in Fig. 2(b). Following observations were noted; (i) P_{FAIL} was found to increase linearly with decrease in L_{PSJ}. (ii) Among all the device variations, highest P_{FAIL} was observed for PSJ-FET with u-GaN in the gate-drain region (iii) PSJ devices with Si substrate exhibited higher P_{FAIL} than those on sapphire. Low P_{FAIL} at larger L_{PSJ} is due to: (i) localization of peak electric field closer to the drain edge, at high L_{PSJ} [6] which enhances impact ionization rate and triggers early avalanche. (ii) Higher R_{ON} and higher thermal resistance from longer drift region increases self-heating in device. (iii) Enhanced carrier trapping in the larger drift area

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accelerates trap driven degradation as discussed in next section. Broader SOA boundary observed in PSJ-FET is attributed to the improved device robustness in presence of super junction. The u-GaN/AlGaN/GaN material stack present in PSJ-FET gives rise to lateral super junction. The embedded super junction in GaN FET has following advantages; (i) It suppresses current collapse. (ii) It offers linear potential distribution and 'box-like' field profile in drift region which enhances device breakdown voltage [6]. This improves device robustness and widens the SOA boundary by 40 percent as compared to conventional HEMT. As seen in Fig. 2(b), the device with u-GaN only in gate-drain region showed highest P_{FAIL}. It highlights that the position of super-junction in PSJ-FET also influence device reliability and is discussed in detail in next section.

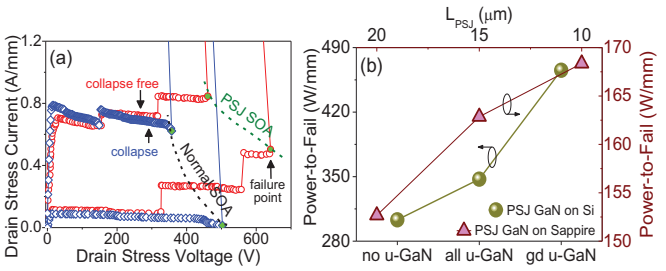

Figure 2. (a) Comparison of Pulsed I–V characteristics depicts that PSJ GaN FET remains collapse free and exhibits a broader SOA boundary when compared with conventional GaN HEMT. (b) Power-to-Fail (P_{FAIL}), normalized to 1mm of device width, as a function of super junction length for devices w/ and w/o u-GaN. Device with u-GaN, exclusively in the gate-drain region (gd u-GaN), show maximum ruggedness i.e. highest P_{FAIL}. P_{FAIL} increases linearly when L_{PSJ} was decreased.

IV. Trap Induced Degradation

To understand the influence of polarization junction's position within source-drain region, on device robustness, devices were tested (i) with p-GaN/u-GaN all over source-drain region (all p-GaN/u-GaN), (ii) p-GaN/u-GaN in only gate-drain region (gd p-GaN/u-GaN) and (iii) without p-GaN/u-GaN (no p-GaN/u-GaN). Also, to understand the influence of substrate on device performance, device realized on Si and sapphire substrate were characterized. In each case, linear drain current was measured after each pulse, to monitor degradation. Figure 3 shows the degradation recorded in spot measured drain current during high current stress, in all three types of devices. A unique degradation trend was observed in each case. As depicted in Fig. 3(a), FET on Si degraded in stepwise manner while FET on thick sapphire degraded gradually as shown in Fig. 3(b). The corresponding pulsed I-V characteristics are shown in Fig. 3(c)-(d). As clear from Fig. 3(a), the absence of p-GaN/u-GaN from gate-drain drift region induced current collapse. The percentage collapse in drain current increases linearly with drain stress as shown in Fig.3(c)-Inset. Possibly, RIE etching of p-GaN and u-GaN in drain drift region, created additional surface states which led to current collapse [9]. Further, the device with p-GaN/u-GaN present all over source-drain region, showed early failure. Therefore, a device with p-GaN/u-GaN only in gate-drain region, was found more robust than other two device types. The effect of substrate on device performance is also evident from difference in I-V characteristics as shown in Fig. 3(c) and Fig. 3(d). As seen in inset of Fig. 3(d), device on sapphire substrate offered higher R_{ON} and early current saturation than device on Si. Possibly, lower thermal conductance of thick sapphire enhances the channel temperature which degrades the carrier mobility. This observation confirmed that substrate can limit device performance. It is worth mentioning that, influence of intrinsic defects/trap originating from buffer/substrate mismatch also play significant role here. Degraded mobility also resulted in R_{ON} increase and increment in the associated self-heating. Ultimately, at high stress current, the device sees thermal runaway like failure as confirmed by post failure analysis. It is possible to reduce the thickness of the sapphire to achieve effective thermal management [4].

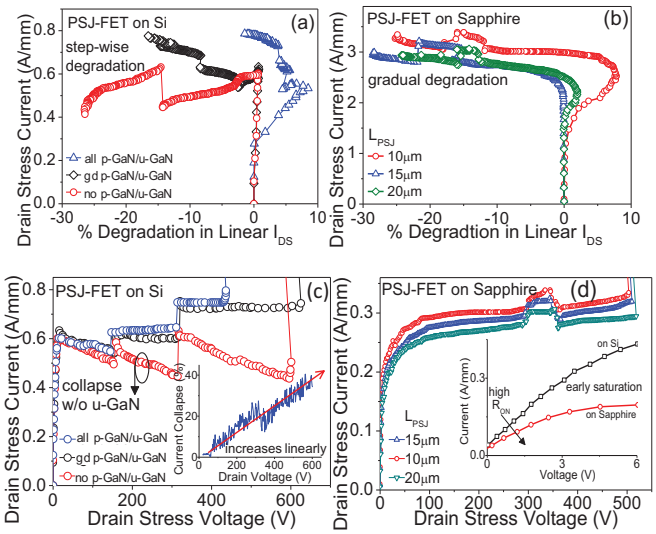

Figure 3. Degradation in drain current, spot measured after each stress pulse applied across devices while conducting pulsed I-V based SOA measurements. (a) PSJ-FET on Si substrate degrades in stepped manner while (b) PSJ-FET on sapphire undergoes gradual degradation. Trap induced degradation seems dominant in PSJ-FET on Si. However, higher self-heating in PSJ-FET on sapphire potentially shadows the effect of trapping on the device degradation. (c) Absence u-GaN layer from gate-drain drift region is observed to induce current collapse which increases linearly with drain voltage (Inset). (d) ON-state behaviour of PSJ-FET on Sapphire. Low thermal conductivity of sapphire increases channel temperature and degrade carrier mobility which increase R_{ON} (Inset).

V. Degradation Physics

To understand the failure mechanisms under ON and OFF state, complete dc characterization of device was done at regular intervals during the test. To begin with, a device was stressed under pinch-OFF conditions at 100 ns pulse width and its dc I-V and C-V characteristics were recorded at different stress levels. Figure 4 shows the corresponding results from intermediate dc characterization. As depicted in Fig. 4(a), device failure under OFF-state stress was found to occur with partial increase in drain-source leakage current accompanied with negative threshold voltage shift. This can be explained as follows: In PSJ-FET there exists an inherent PN body diode formed by 2DHG/2DEG. The voltage stress at drain, reverse biases the inherent PN and depletes the AlGaN drift region. At higher stress voltage, holes are generated at drain end due to

impact ionization. Excess holes are swept towards the lowest potential and on the way are collected by the gate, under the influence of field of reverse biased PN junction. This constitutes increased gate current on the verge of breakdown as shown in Fig. 4(b). Also, the energetic holes can damage the interfaces underneath gate and/or get trapped in gate region. This additional charge under gate introduces V_{TH} shift as observed in Fig. 4(a). Figure 4(c) shows the variation recorded in the total gate capacitance profile with drain stress, in subthreshold regime. The change in gate capacitance confirms carrier trapping in regions underneath gate (p-GaN/u-GaN/AlGaN). Figure 4(b) shows the variation in gate leakage with drain stress. Instability can be observed in gate current at the verge of catastrophic failure. This is possibly due to the formation of defects at high stress, in and underneath gate stack. On the verge of device failure/breakdown, gate leakage increases to same order as OFF-state drain-source current. This observation highlights that the gate current increases due to introduction of drain-to-gate leakage via the percolation path(s) which were formed by increased defect density in gate stack with stress. Figure 4(d) shows degraded output characteristics of the device. The reduced I_{ON} possibly results from trapping in the AlGaN barrier and at AlGaN/GaN interface, which increases R_{ON}. Under ON-state, voltage drop across channel, lowers the potential underneath JFET region, formed by PSJ (Fig. 1b). This increases strength of reverse bias and depletion width across JFET [7], which shrinks the effective conduction area to enhance local current density at PSJ edge. High current density with peak electric field, enhances power density and cause hotspot formation at PSJ edge, which leads to thermal failure as confirmed by post failure analysis. Therefore, ON-state failure is thermally driven and exhibits power dependence while OFF-state failure involves impact ionization and shows field dependence. Unlike in OFF-state stress, under ON state, gate and drain-source leakage remained intact until the device failed abruptly, which is another signature of the thermal failure [8]. It was found that the vertical buffer leakage did not change under both ON and OFF state stresses, which implies absence of buffer degradation, unlike in conventional HEMT [10], where dominant avalanche-injection mechanism triggers impact ionization in buffer causing failure.

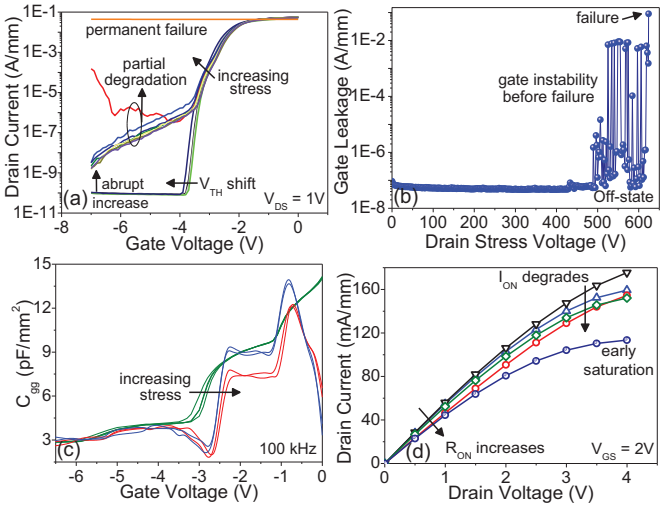

Figure 4. (a) Partial increase in DC OFF-state drain-source current with negative shift in threshold voltage, measured in between high current stress at the drain. It highlights (b) deteriorated gate control with increase in gate leakage post stress. Instability is observed in gate current at the verge of catastrophic failure, due to the formation of defects in and underneath gate stack as also indicated by (c) altered gate capacitance in sub-threshold regime. (d) Fall in drain current with increasing stress reveals trapping in the AlGaN barrier and at AlGaN/GaN interface which leads to increased R_{ON}.

VI. Unique Failure Modes

To gain physical insight into the underlying failure mechanism, failure analysis of damaged devices was done using Scanning Electron Microscopy (SEM) and Energy Dispersive X-Ray Spectroscopy (EDX). In all the devices, the top SiO_2 passivation was blown-off from damage area.

Figure 5(a) shows SEM micrograph of PSJ FET which failed when stressed under OFF-state. Multiple damages can be seen along the gate edge towards source. The source edge also got roughened as seen in SEM image. EDX analysis confirmed presence of Au in damage location. The gate failure observed under OFF-state stress with multiple damages in gate-source region, corroborates well with the degradation mechanism explained in section V, where holes generated due to impact ionization are suggested to degrade the gate stack. Moreover, on the verge of failure, possibly the hot spot present at the gate edge led to the melting of Au from gate, followed by its migration and accumulation on source edge which eventually roughened it as seen in Fig. 5(a). SEM micrograph in figure 5(b) shows device which failed under ON-state stress. It reveals that the device failed with a crack running across the source-drain region. Another device failed in ON-state with bulging of GaN film as depicted in Fig. 5(c). The cracking and bulging of GaN film in gate-drain region are thermally driven. This can be verified from the fact that gate finger melted exclusively at the damaged locations as seen Fig. 5(b)-(c) and highlights the thermal stress driven failure in PSJ-FET under high drain current stress. The failure analysis of PSJ-FET reveals that failure occurs in source-gate region under OFF-state and in gate-drain region under ON-state stress. Moreover, failure under OFF-state is field driven whereas ON-state failure is thermally driven. Figure 5(d) shows post failure SEM micrograph of conventional HEMT which failed under ON-state. It reveals presence of crack which originated from drain side gate edge. In AlGaN/GaN HEMT, the peak electric field at the drain side gate edge induces piezoelectric strain in gate vicinity [11] which possibly damaged the gate finger and created defects in gate-drain region. At high drain voltage, the hot electrons get trapped in these freshly formed defects [12] and eventually caused device failure.

VII. Conclusion

PSJ-GaN FET exhibited broader SOA boundary than conventional HEMT. SOA robustness (Power-to-Fail) showed linear dependence on PSJ length. Presence of u-GaN, in drift region, mitigated current collapse and improved SOA boundary. Unique device degradation trends and their implications on device failure, both under ON and OFF states, were studied. Lower thermal conductivity of substrate was found to limit SOA boundary due to enhanced self-heating.

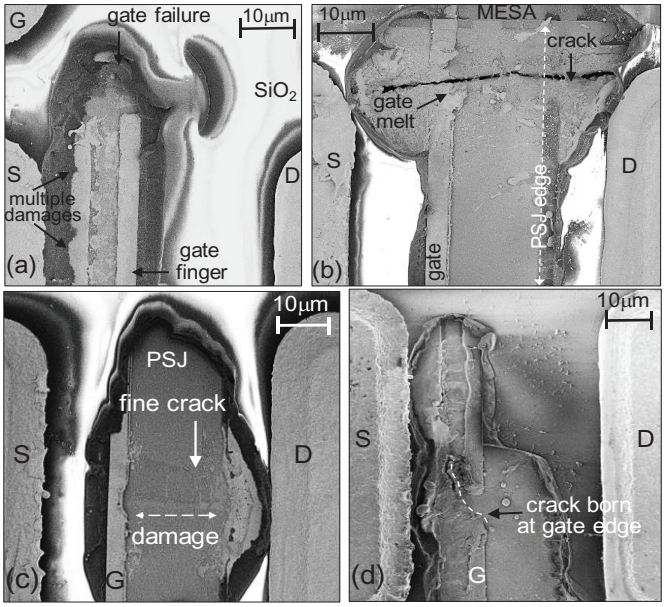

Figure 5: (a) SEM micrograph of PSJ FET failed under OFF-state. Multiple damages along gate edge towards source can be seen. Source edge roughened due to Au deposition from gate edge as confirmed by EDX. SiO_2 passivation peeled-off from failure locations. (b)-(c) Post failure SEM micrograph of PSJ FET which failed under ON-state. (b) Figure shows crack from source to drain. Melting of gate finger exclusively at cracked location indicates thermal stress induced cracking at high drain current. (c) Damage in gate-drain drift region is visible. Gate metal curls/folds at damage spot which points to high temperature induced melting at high drain current stress. Fine cracks in the PSJ region were also seen. (d) SEM micrograph of conventional HEMT which failed under ON-state. Figure reveals crack originated from drain side gate edge where lateral electric field peaks.

OFF-state failure was attributed to gate stack degradation while ON-state failure was thermally driven due to hotspot formation at the PSJ edge. Conventional HEMT like buffer degradation was missing in PSJ GaN FET.

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