Proceedings of the 31st International Symposium on Power Semiconductor Devices & ICs
May 19-23, 2019, Shanghai, China

Performance and Reliability Co-design of LDMOS-SCR for Self-Protected High Voltage Applications On-Chip

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Abstract— **In this work we address turn-on vulnerability of conventional LDMOS-SCR devices under standard circuit operation window. This behavior is correlated with early ESD / SoA failure and power-to-fail scalability issue in HV LDMOS-SCR devices. The 3D TCAD is used to Develop physical insights into the performance and reliability limiters of LDMOS-SCR device. Different engineered designs are proposed to mitigate turn-on vulnerability and ESD power to fail scalability, while keeping channel performance and hot carrier degradation unaffected.**

***Index Terms*—Electrostatic Discharge, Laterally Double Diffused MOS (LDMOS), Silicon Controlled rectifier (SCR).**

I. INTRODUCTION

LDMOS devices are used to implement high voltage (HV) circuit functionalities in System on Chips (SoCs), Power SoCs (PwrSoC) and automotive ICs. Given the exposure of these HV applications to outside world and extreme conditions, LDMOS devices in these functionalities are often prone to early ESD damage. This is known to be attributed to space charge modulation induced current filament formation [1-2]. An embedded parasitic SCR in LDMOS (LDMOS-SCR) is proposed to have higher ESD robustness, which is a potential contender for self-protected HV applications [3-4]. However, it's failure under longer time electrostatic discharge – common in automotive environments – is still a major concern [5]. Besides, these devices can have functional SCR turn-on. These two issues hinder its self-protection capability and circuit functionality, respectively. This work for the first time attempts to provide physical insights into these issues. Moreover, this work provides physics-based device design to address these keeping channel performance and hot carrier reliability unaffected.

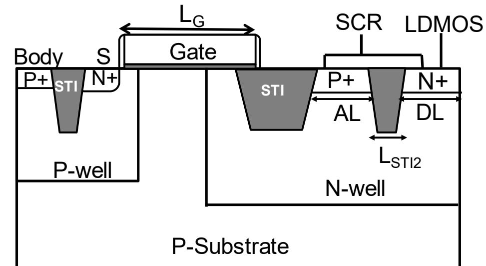

Fig. 1: Cross-sectional View of conventional LDMOS-SCR. To extract intrinsic LDMOS characteristics of LDMOS-SCR design, P+ (in N-Well) terminal was left floating.

II. FUNCTIONAL TURN-ON ISSUES IN CONVENTIONAL DESIGN

The conventional LDMOS-SCR designs as depicted in Fig.1, when used as MOS switch, found to have SCR turn-on at high gate voltages (Fig. 2a & 2b) as signified by jump in drain current in I_D-V_D and loss of gate control in I_D-V_G characteristics. In presence of early SCR turn-on, the I-V characteristics drift away from the intrinsic LDMOS characteristics (Fig. 2c). The intrinsic LDMOS characteristics are obtained by not making a contact to the P+ island in the N-well. The SCR turn on in the device functional region is attributed to accumulation of channel injected electrons in the N-well region below P+ contact, before they reach N+ drain terminal. This results in early SCR action (Fig. 3), Which hinders device's usability as a switch or amplifier. A flipped configuration is proposed to address the SCR turn-on in the

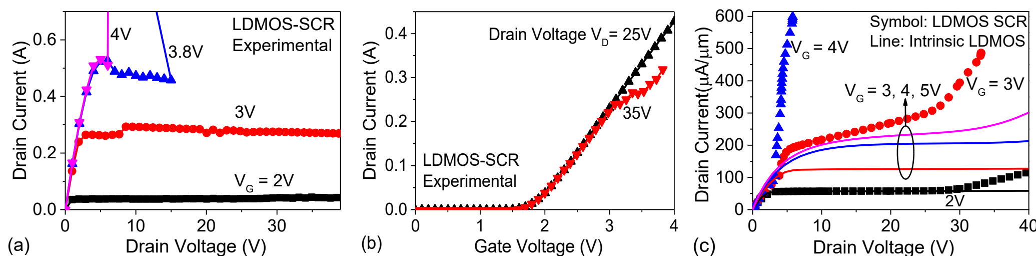

Fig. 2 (a) Measured DC I_D-V_D characteristics of LDMOS-SCR depicting an early SCR turn-on during the functional region. (b) Measured I_D-V_G characteristics show fall in drain current with increase in drain voltage, which is unlikely in intrinsic LDMOS. This is attributed to partial loss of gate's control once SCR is turned-on. (c) Simulated DC I_D-V_D characteristics of LMDOS-SCR depicting presence of strong SCR turn-on and its comparison with I_D-V_D characteristics of intrinsic LDMOS device.

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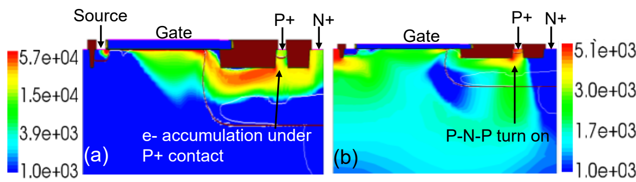
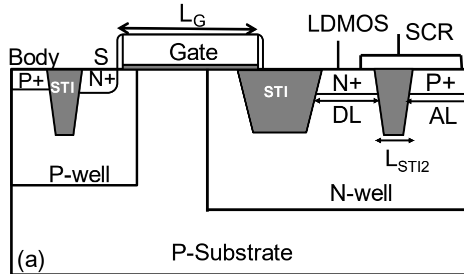


Fig. 3 Electron and hole current densities extracted at V_{GS}= 3V and V_{DS}=30V. Flooding of the gate induced electrons is observed under the P+ (in N-Well) contact, turns-on the parasitic SCR in the functional region.



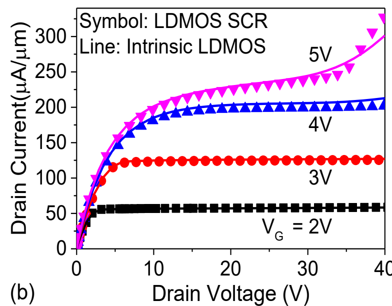


Fig. 4 (a) Cross-sectional view of flipped LDMOS-SCR device which suppresses early SCR action. Position of the N+ Drain and P+ contacts in the N-well are swapped in flipped device. (b) DC I_D-V_D characteristic of the LDMOS-SCR compared with intrinsic LDMOS characteristics confirms absence of SCR action in the functional region.

functional region. Position of the N+ and P+ diffusions in N-well are interchanged (Fig. 4). Proposed flipped configuration found to recover the MOS action by suppressing the PNP turn-on (Fig. 5). The electrons in the N-well are collected efficiently by N+, before they accumulate underneath the P+. However, such a weakening of the PNP action results in severe power scalability issue, as depicted in Fig.6.

III. Power Scalability Problem

LDMOS-SCR devices, when used in automotive applications, can experience longer ESD discharges than the qualified 100 ns duration pulses [5]. The duration of these discharge depends on RC lines for which the high voltage I/O are connected. LDMOS-SCR is stressed with pulses of different duration, using a high impedance load Transmission Line Pulse (TLP) system. As depicted in Fig.6, LDMOS-SCR survives the snapback and fail at high current when stressed with pulse widths less than 100 ns. For longer pulse times (>100ns), device was found to fail at the verge of snapback (increase in leakage is depicted in fig.6(b)). As a result, the

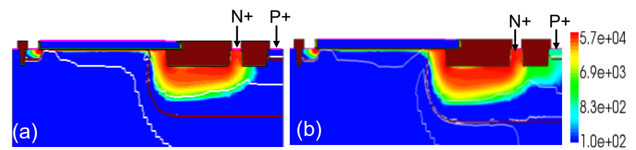
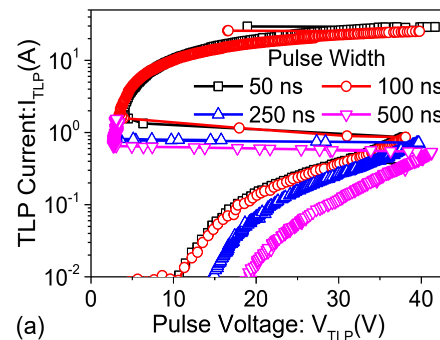


Fig. 5: (a) Electron current density across flipped LDMOS-SCR device extracted at (a) V_D=30 V and V_D=40 V for maximum gate voltage (5V). Gate induced electrons in the N-well are effectively collected by the N+ Drain contact before they accumulate under the P+ contact at higher drain voltage. This phenomenon shifted the onset of SCR turn-on in flipped device beyond device's operating I-V window, mentioned parameters are the knob to tune the performance and voltage rating of the device.

failure current and failure power do not follow expected power law curve as depicted in Fig.7. The device failure is also found to be specific to a window between the snapback and holding current, above which device survives failure. 3D TCAD simulations are used to understand the unique failure physics near the snapback region. The transient lattice temperature plotted for different injected current reveals (Fig. 8) unique device behavior. At low current, device temperature increases linearly with time. At currents near the snapback region, lattice temperature increases above a critical value (Fig. 8), which leads to device failure due to filament induced hotspot formation as depicted in Fig.9. It is observed that majority of the current is collected at N+ contact in the N-well, hotspot is observed underneath the N+ in N-well.



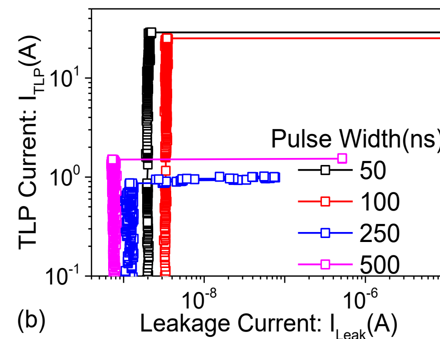


Fig. 6: (a) Measured TLP I-V characteristics of LDMOS-SCR device for different stress pulse widths in grounded gate configuration (b) Leakage current measured after each pulse. Device stressed beyond 100ns duration are observed to fail during the voltage snapback region. The observed failure is found to be specific to window of current near the snapback region.

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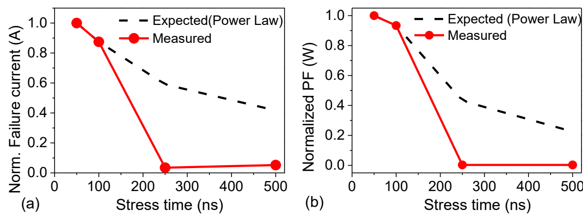

Fig. 7: (a) Normalized Failure current (Norm. with I_{Fail} @ 50ns) and (b) Norm. power to fail extracted at different stress times. The LDMOS-SCR device has shown a sudden fall in failure current from 25A at 100 ns to 1.5 A for 250 ns, depicting severe power-to-fail scalability issues. The expected failure current scaling according to the power law behavior is plotted in the same graph.

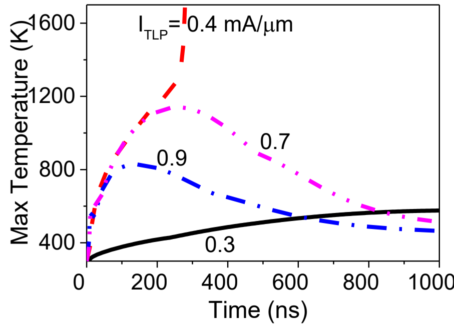

Fig. 8: Maximum lattice temperature as a function of stress time in flipped LDMOS-SCR device for different injected TLP currents, in the low current snapback region. For smaller currents lattice temperature increases linearly with time, for medium current levels, the lattice temperature increases exponentially leading to peak temperature above failure temperature. However, with increasing TLP current the temperature falls to lower values after reaching a maximum. A unique device failure is visible in a window of currents.

With further increase in injected current, the magnitude of peak reduces and time at which the peak appeared shift to lower time scales (Fig.8). This is attributed to faster turn-on of the parasitic SCR (Fig.10) at higher injected currents. This allowed current spreading, mitigated device heating and allowed device to survive failure at high currents (Fig.10). Majority of the current is observed to be collected by P+ in the N-well, shows the SCR turn on (Fig.10). Different physical events are summarized in fig.11.

IV. Design Solutions

Two physics-based design solutions are proposed to modulate the P-N-P and or SCR turn on time. (1) Reducing N+ drain diffusion length DL. This weakens the LDMOS action, increases electron accumulation in N-well and leads to faster SCR turn on (Fig.12). Faster SCR turn-on reduces the lattice temperature near the snapback causes safe snapback. (2) Increasing AL too lowers the SCR turn-on time, which is due to increase in emitter area (Fig. 13). These two designs yielded power law behavior or power-to-fail scalability (Fig. 12c & 13c). While increasing AL doesn't affect channel performance and hot carrier reliability, DL reduction was found to improve channel performance (Fig.14) and increase Hot carrier degradation (Fig.15).

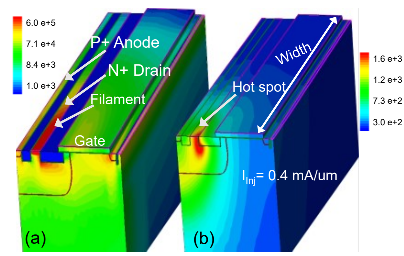

Fig. 9: (a) Current density (A/cm²) and (b) lattice temperature (K) for an injected current density of 0.4 mA/μm, extracted at 250ns. Filament induced hotspot causes device failure. The Parasitic SCR is not triggered in this case. Majority of the current being collected by N+ drain contact, not by P+ contact, depicting absence of SCR action.

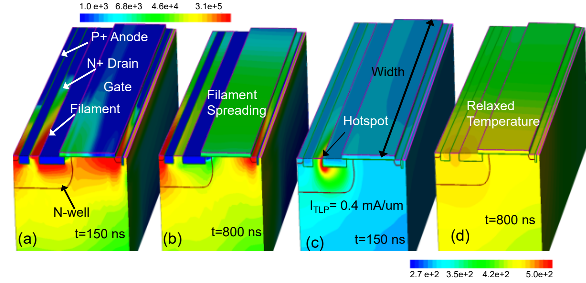

Fig. 10: (a) – (b) Current density (A/cm²) and (c) – (d) lattice temperature (K) extracted at different times: (a,c) 150ns & (b,d) 800ns, for an injected current of 0.9 mA/μm. (a,c) Absence of SCR turn-on (before device failure) leads to filament driven hot spot formation and device failure. (b,d) Fast PNP turn-on at higher currents enables SCR turn-on before LDMOS driven filament failure. This allows filament to spread and avoids early failure.

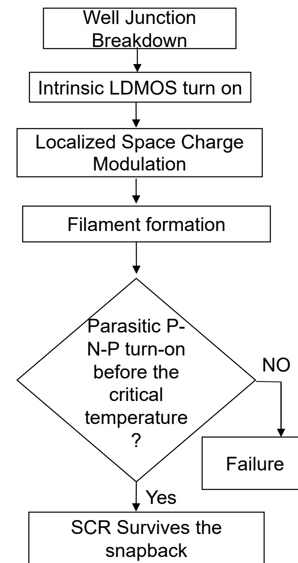

Fig. 11: various physical events responsible for poor power scalability in LDMOS-SCR.

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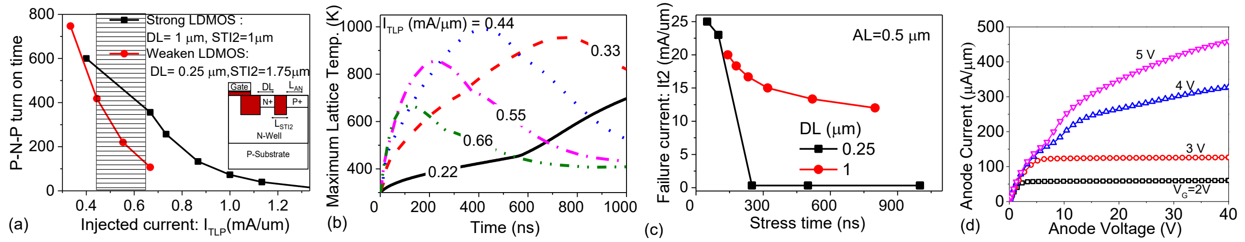


Fig. 12 (a) Comparison of SCR's _P-N-P turn-on time in LDMOS-SCR device in flipped configuration for different DL. By lowering DL, to reduce collection of electrons from N-Well, SCR turn-on gets strengthened. This is because of accumulation of electron in N-Well, which trigger SCR's parasitic PNP faster. (b) Temperature profile for different injection currents when DL was reduced. (c) Power scalability recovered with improved SCR action. (d) Output characteristics slightly deviate from the intrinsic LDMOS.

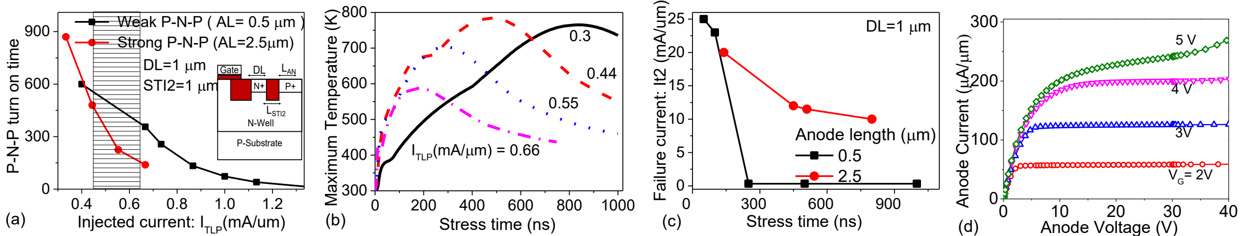


Fig. 13: (a) Comparison of SCR's P-N-P turn-on time in flipped LDMOS-SCR device configuration for different SCR strengths while keeping intrinsic LDMOS intact. By increasing P+ length (AL) SCR and PNP turn-on was strengthened. (b) Temperature profile for different stress currents when intrinsic PNP strength was enhanced by increasing AL. (c) Power scalability recovered when SCR's parasitic PNP turn-on was improved by increasing AL. (d) Output characteristics of device with increase AL.

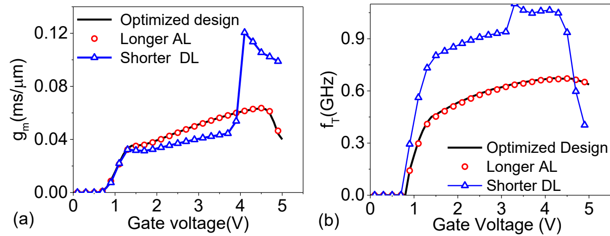
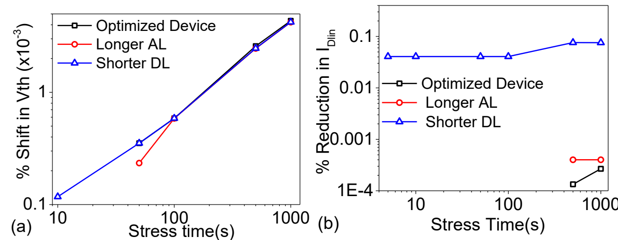


Fig. 14: (a) Transconductance, (b) cut-off frequency and (c) Gate to drain Capacitance of three different designs.



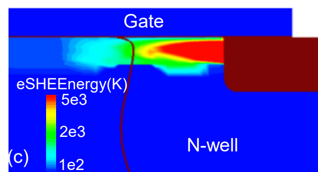


Fig. 15: Comparison of threshold voltage and linear drain current shift with stress duration for three different designs under stress. Shorter DL device found to has higher degradation in Idlin. (c) Electron Hot carrier energy.

V. Conclusion

The conventional LDMOS-SCR devices are found to be vulnerable for SCR turn on in the functional region attributed to high electron density under the P+ region in N-well. The engineered flipped device configuration can mitigate the SCR turn on because of weak P-N-P action. However, such design suffers from Power scalability issues when TLP stressed with long duration pulses. The inherent LDMOS forms filament due to the non-uniform space charge modulation near the snapback region and causes device failure. When stressed with higher current, the SCR turns on before the filament temperature reaches critical value, causes filament spreading and hotspot reduction. The proposed design solutions, where increasing AL and reducing DL have yielded improved power scalability in flipped designs. A reduction in DL causes more electron accumulation in N-well contributes to faster SCR turn on. Increasing AL implies larger emitter area of P-N-P that leads to improved SCR turn on time .

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