Impact of Space Charge Modulation on Superjunction-LDMOS

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ABSTRACT

In this paper, we present the impact of Superjunction (SJ) implant on the performance challenges encountered by LDMOS in the ON-state while developing insights into Space Charge Modulation (SCM) and Quasi-Saturation (QS) behavior in these devices. SJ-device is reported to have four times higher breakdown voltage than the conventional LDMOS device which proves to be an outstanding candidate for switching applications. This paper elucidates the design guidelines for SJ-devices in order to maximize the ON-state performance by mitigating SCM and QS effects while keeping in mind the OFF-state breakdown requirements.

INTRODUCTION

Incessant advancement in the processing technology has led to the introduction of integrated high-performance lateral double-diffused MOS (LDMOS) transistors, which has fueled the development of power system-on-chips (SoCs) [1]. Besides, these LDMOS transistors are extensively used in high-power switching and RF applications in advance system-on-chips [2], [3]. Achieving a low on-resistance (R_{ON}) while sustaining high breakdown voltage (V_{BD}) has always been a challenge in designing such high voltage devices. One of the most effective and recently reported ways is the introduction of Superjunction (SJ) implant in LDMOS devices to create SJ effect in the drift region, which widens the depletion region in the OFF-state and extends the V_{BD} limit [4]-[6]. Nevertheless, under high current operation, LDMOS devices conduct with high carrier density over a lightly doped drift region resulting in space charge modulation (SCM) [7]. This effect is often ascribed to the onset of quasi-saturation (QS) which affects the transistor operation as well as its safe operating area [8], [9]. Earlier works reported implications of SJ-implant on the switching characteristics of LDMOS, however its impact on the SCM and QS is least explored. This work attempts to fill this gap while developing the required physical insights and design guidelines.

DEVICE PHYSICS AND ONSET OF SCM

SJ-LDMOS is designed with a p-type implant (P-top) in the n-type drift region at the surface (D_{Ptop}=0) (Fig.1(b)) and away from the surface (D_{Ptop}>0) (Fig.1(c)). These device variants are designed over a process calibrated setup of 0.18µm BiCMOS foundry. The device performance is studied using a well-calibrated TCAD setup [10].

OFF-State Behavior

SJ-LDMOS with D_{Ptop}>0 allows maximum space charge distribution in Nwell compared to the SJ-LDMOS with D_{Ptop}=0 (Fig. 2(a)). For D_{Ptop}=0, the peak electric field resides near the Ptop-Nwell junction at the surface which expands to the overlap region of gate-Nwell (L_{OV}) and so, the critical electric field at the surface (Fig. 2(b)). Whereas for D_{Ptop}>0, the electric field peaks at Ptop-Nwell junction away from the surface which results in more uniform distribution of electric field (Fig. 2(c), (d)). Therefore, positioning of SJ in the drift region plays a vital role in determining the breakdown performance of the device. Furthermore, there is 4x improvement in the V_{BD} without trading of the R_{ON} (Fig. 1(d)). It is worth highlighting that, SJ is design-optimized over a fixed layout footprint of the conventional LDMOS (Fig. 1(a)), therefore maximizes the $R_{ON\text{-}Sp}$ performance.

ON-State Behavior

At higher gate voltage, the current density in the LDMOS drift region exceeds background doping. As a result, peak electric field shifts from the gate to the drain edge of the device (Fig. 3(a), (b)). In case of SJ implant with D_{Ptop}=0, current conduction is restricted to the path under the implant. Therefore, onset of SCM is enforced by the shift in electric field close to the lower edge of Ptop-Nwell junction towards drain (Fig. 3(c)). On the other end, where D_{Ptop} >0, a significant fraction of current conducts through the surface of the drift region. Moreover, retrograde doping of high voltage Nwell is depleted across the SJ implant, causing higher current crowding in D_{Ptop}>0 when compared to D_{Ptop}=0. Also, due to surface conduction, the significant current crowding near drain attributes to the early onset of SCM. When V_{DS} increases further, high electric field at drain contact followed by SCM causes an excessive carrier generation due to avalanche multiplication resulting in an increased current density in the drift region (Fig. 3(e)). This sequentially leads to high impact ionization near drain edge causing reduction in the ON-state breakdown of the device which severely affects device safe functional area. Because of well-distributed current in the drift region, SJ-LDMOS with D_{Ptop}=0 offers better electrical characteristics than D_{Ptop}>0 (Fig. 4 (a), (b)). Also, an early QS adversely impacts the transconductance (g_m) since, the g_m-reduction occurs at lower gate voltage, reducing the maximum allowed gate swing in D_{Ptop}>0 (Fig. 4(c)). Also, as soon as QS occurs, severe non-linearity follows in miller capacitance (C_{GD}) (Fig. 4(d)). This restricts the device performance in analog and RF applications.

DESIGN GUIDELINES FOR SJ-DEVICE

While designing SJ-LDMOS, design parameters such as P-top implant doping (N_{Ptop}), thickness (H_{Ptop}), projected range (D_{Ptop}), distance from the gate edge (L_{PG}) and from the drain edge (L_{PD}) are considered for the design of experiments (DOE). N_{Ptop} and H_{Ptop} are codependent. As N_{Ptop} increases, V_{BD} increases with effective surface field reduction due to maximum dose balance. However, higher N_{Ptop} creates a weak site at drain contact, causing early breakdown (Fig. 5). Besides this, D_{Ptop} is crucial in defining SJ-device design limits. For shorter D_{Ptop}, the depletion region reaches out to the drain first and then to surface which causes a significant carrier crowding near drain leading to early SCM/QS. Whereas for larger D_{Ptop}, the critical electric field is held at gate-Nwell overlap edge. Since most of the charge carriers drift through surface, the advantage of dual conduction path is compromised for larger D_{Ptop} values (Fig. 6). Similar to this is the effect of L_{PD} which when increased results in suppressed electric field localized at drain and thus, mitigating early onset of SCM and QS.

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CONCLUSION

SJ-device offers 4x higher breakdown voltage when compared to the conventional LDMOS for a given layout footprint. As a result, a better $R_{ON\text{-}Sp}$ vs V_{BD} is traded. Furthermore, SJ implant doping and placement determine the effective design of surface field reduction while offering high voltage functionality. However, it suffers from early SCM/QS due to reduced drift area and increased current density. ON-state breakdown with respect to SJ imposed early QS is correlated. Moreover, SJ implant limitation addressing early SCM/QS highlights the design guideline for maximizing the device safe functional area.

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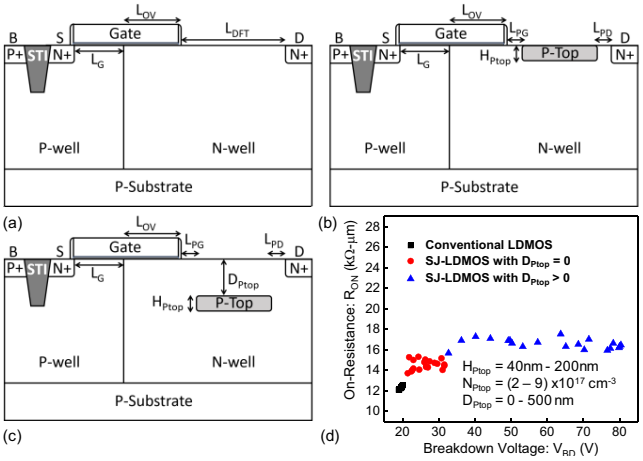

Fig. 1. Schematic of (a) Conventional LDMOS, (b) SJ-LDMOS with D_{Ptop}=0, and (c) SJ-LDMOS with D_{Ptop}>0. (d) Comparison of R_{ON} versus V_{BD} trade-off for a range of H_{Ptop}, N_{Ptop} and D_{Ptop}. Design parameters, L_G: Channel Length and L_{DFT}: Drift Length.

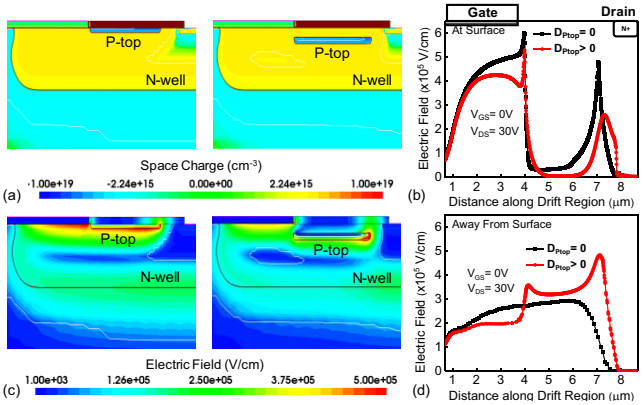

Fig. 2. (a) Space charge, & (b) Electric field comparison of SJ-LDMOS. Electric field profile along drift region for the two SJ-LDMOS (c) at the surface, and (d) 400nm away from the surface.

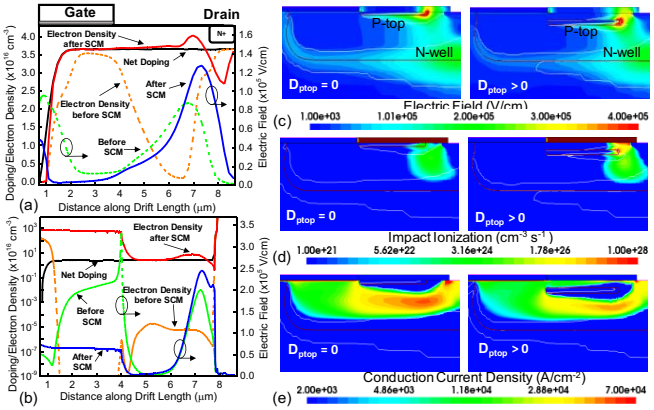

Fig. 3. (a) and (b) Net doping concentration, electric field and electron density along the drift region depicting space charge modulation in SJ-LDMOS with D_{Ptop}=0 and D_{Ptop}>0, respectively. (c) Electric field, (d) Impact ionization, and (e) Conduction current density after SCM.

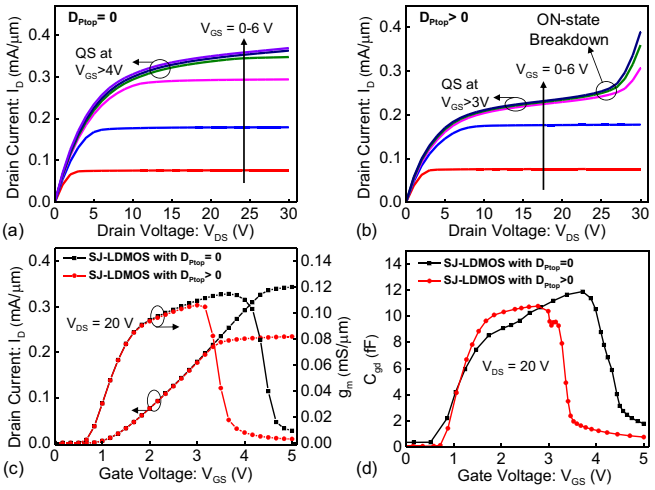

Fig. 4. Simulated output characteristics of SJ-LDMOS with SJ-Implant at (a) D_{Ptop}=0, and (b) D_{Ptop}>0 for V_{GS} values of 0V, 2V, 3V, 4V, 5V and 6V. (b) Comparison of I_D-V_{GS} and g_m-V_{GS}, and (d) C_{GD}-V_{GS} characteristics for V_{DS}=20V.

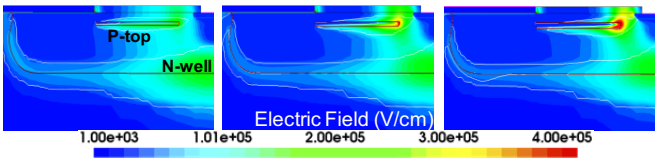

Fig. 5. Electric field distribution at higher drain voltage with increase in N_{Ptop} from 4x10^{17}cm^{-3} (left) to 6 x10^{17}cm^{-3} (right).

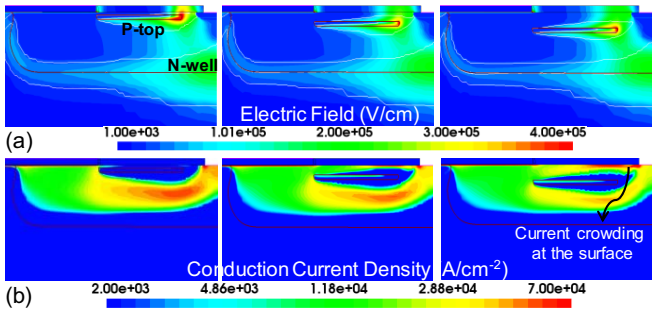

Fig. 6. (a) Electric Field distribution, and (b) Conduction Current Density with increase in D_{Ptop} from 100 nm (left) to 500 nm (right).

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