On the Root Cause of Dynamic ON Resistance Behavior in AlGaN/GaN HEMTs

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Abstract— **Channel field and stress time dependent critical voltage in dynamic ON resistance of GaN HEMTs is reported for the first time. Electro – Photo Luminescence, low temperature stress experiments and their dependence on device parameters is correlated to propose a novel channel field and buffer trap interaction mechanism regulating the critical voltage which is not related to new trap generation or hot electrons.**

Index Terms— **Dynamic ON Resistance (R_{ON}), AlGaN/GaN HEMTs, Critical voltage, GaN buffer traps, Electro-luminescence (EL)**

I. Introduction

Despite their wide scale acceptance as power and RF devices, reliability of GaN HEMTs is a major concern with dynamic ON resistance (DR_{ON}) emerging out as one of the most challenging reliability problems. Several design techniques have been explored in the past to alleviate DR_{ON}, viz., GaN buffer designing [1] – [5], and surface passivation (SiN_x [6], AlN [7], GaN cap [8]). These techniques are based on the understanding that DR_{ON} is caused by trapping of electrons in trap sites located in GaN buffer or device surface. However, a detailed study on transport mechanism to these trap sites and its dependence on electric field is missing. In this work, we report a critical voltage for DR_{ON} in AlGaN/GaN HEMTs which is strongly correlated to stress time and electric field redistribution making it a function of device parameters, viz, source to drain length (L_{SD}), field plate length (L_{FP}) & passivation thickness (t_{passi}). Electro (EL) & photo luminescence (PL) studies along with temperature dependent DR_{ON} are correlated to propose an electron transport mechanism from channel to buffer traps.

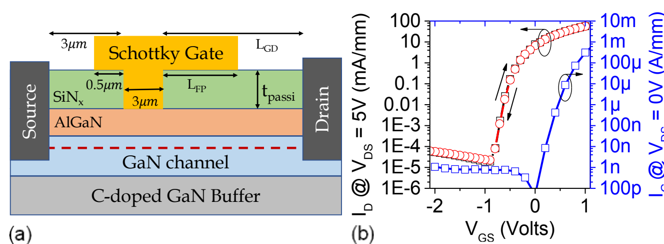

Figure 1. (a) Fabricated Schottky gated AlGaN/GaN HEMT on commercial 600-V stack, (b) Transfer and gate leakage characteristics depicting negligible hysteresis & low leakage current demonstrating excellent surface and interface quality.

II. Device Fabrication and Experimentation

Schottky gated HEMTs were fabricated on 600V commercial grade GaN on Si epistack with different device parameters (Fig. 1a). t_{passi} was varied by controllably etching SiN_x from access regions using O_2-CHF_3 plasma. Processing all dies simultaneously using an optimized process [9] ensured minimal device variability. Negligible hysteresis in transfer characteristics of the device with very low leakage current demonstrates superior interface quality (Fig. 1b). DR_{ON} of the HEMTs was studied by DC stressing the devices [10]. The devices were stressed in OFF state ($V_{GS} \approx V_{TH} - 1.5\,V$) for $100\mu s$, with the drain stress voltage ($V_{DS-Stress}$) varied from 0 to 200V.

III. Critical Voltage and Its Dependence on Device Design

A. Critical Voltage

Fig. 2 depicts DR_{ON} of the device as a function of $V_{DS-Stress}$ for different stress times. It depicts a critical $V_{DS-Stress}$ (V_{cr}) beyond which a drastic increase in DR_{ON} is observed. Further, V_{cr} reduces with increase in stress time. Device recovery to pristine condition post stress experiment (Fig. 3a) suggests that no additional traps are generated. This is also reflected in the PL spectra depicting similar intensity of defect signal corresponding to yellow luminescence (YL) and blue luminescence (BL) bands before and after stress (Fig. 3b). Absence of any EL signal under similar stress conditions suggests minimal hot electron generation. Further, stressing the device in semi-ON state did not result in any significant DR_{ON} (Fig. 3c), establishing V_{cr} to not be defined by hot electrons.

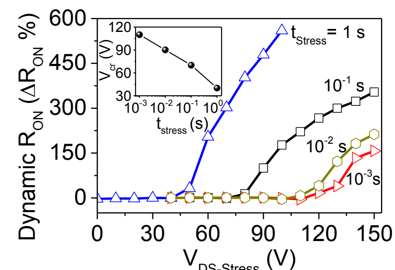

Figure 2. Dynamic R_{ON} of the device as a function of stress voltage with different stress durations. A critical voltage can be clearly seen which reduces as stress duration is increased. $\Delta R_{ON} = (R_{post-stress} - R_{pristine})/R_{pristine} \times 100$.

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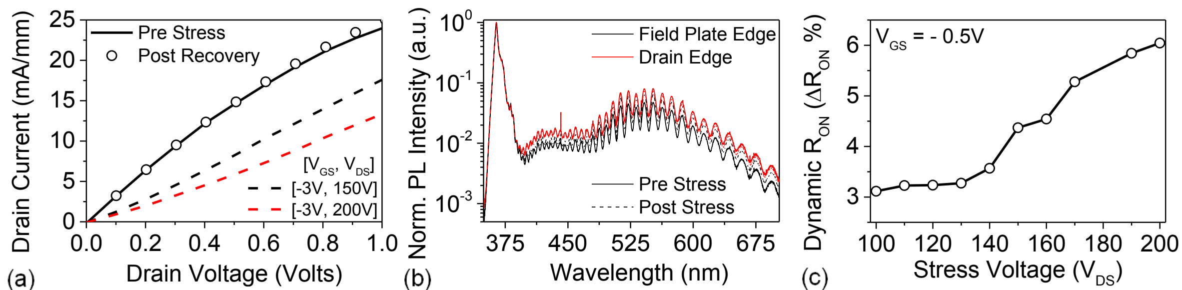

Figure 3. (a) Increase in R_{ON} of the device as a function of drain stress voltage. Post device stressing and recovery with wait time of ~180 s restores the pristine device characteristics. (b) UV PL at field plate and drain edge before and after 200V drain sress depicts similar intensity peaks thereby establishing that stress experiment doesn't result in generation of traps. (c) Dynamic R_{ON} extracted as a function of drain stress voltage when the device was biased in semi-ON condition (favorable for hot electrons) depicts negligible dynamic R_{ON} and an absence of critical voltage.

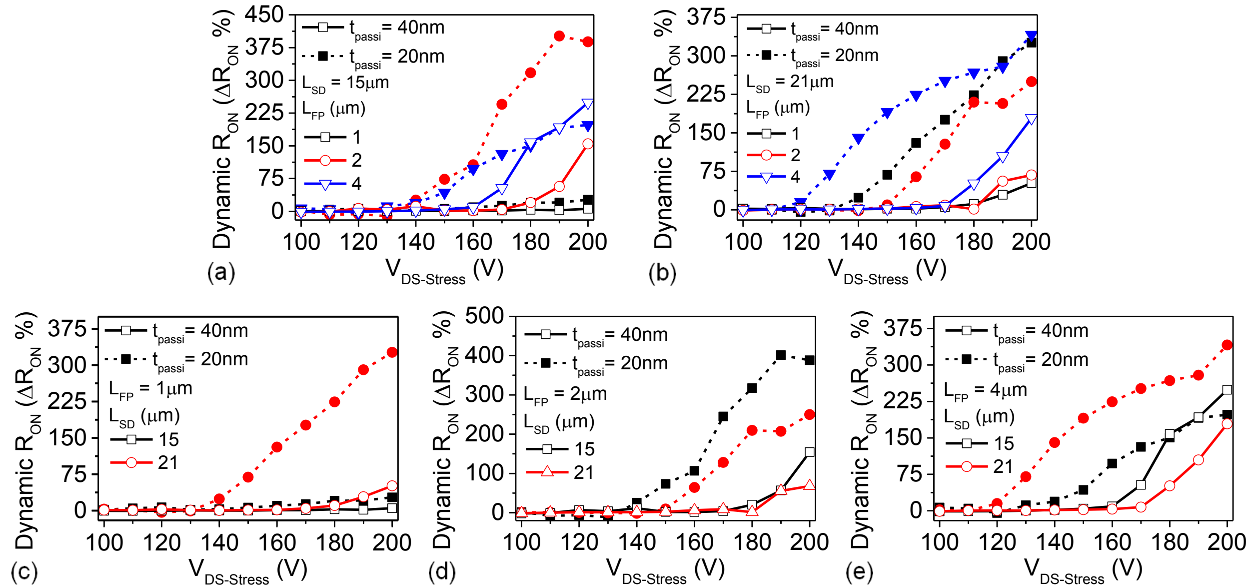

Figure 4. Dynamic R_{ON} extracted for devices as a function of lateral device parameters (i) Variable field plate length (L_{FP}) with L_{SD} as : (a) 15 μm, (b) 21 μm and (ii) Variable source-drain distance (L_{SD}) with L_{FP}as : (c) 1 μm, (d) 2 μm, and (e) 4 μm Figure also compares dynamic R_{ON} for two different passivation thickness. Devices were stressed in OFF state with $V_{GS-Stress} \approx V_{TH} - 1.5$. A clear dependence of critical voltage on lateral device parameters can be observed.

B. What defines critical voltage?

Dependence of V_{cr} on lateral device design parameters suggests channel field dependence of V_{cr} (Fig. 4). Since all the devices had similar surface conditions, the variation in V_{cr} is associated with interaction between channel electric field and GaN buffer. EL analysis of different devices depicts a peak near field plate (FP) edge (Fig. 5), suggesting that interaction between electric field near FP edge and buffer traps plays a key role in determining V_{cr}.

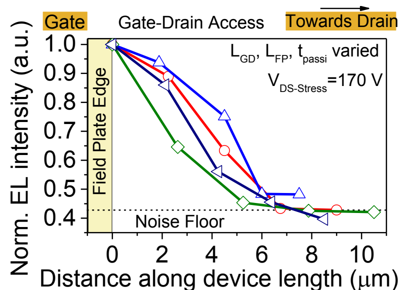

Figure 5. Normalized EL intensity of different devices with critical voltage < 170 V depicting an EL intensity peak near field plate edge.

C. Mechanisms governing V_{cr}

A comparison of PL and EL depicts that for higher $V_{DS-Stress}$, the YL and BL band manifest themselves in the EL spectra (Fig. 6). This indicates that beyond a certain $V_{DS-Stress}$,

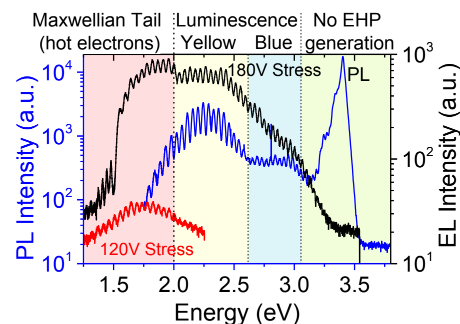

Figure 6. A comparison of PL spectra and EL spectra (extracted at two drain stress voltages) depicts yellow (YL) and blue luminescence (BL) peaks in the EL spectra only at higher drain stress voltages, suggesting that a sufficiently high drain stress is required for hot electrons to interact with defect states in the GaN buffer. YL is attributed to radiative transitions between (V_{Ga}-O_N) shallow donor-deep acceptor complex, Ga_i, N_{Ga}, C_N defects. BL is attributed to C_{Ga} donor- C_N acceptor pair transitions.

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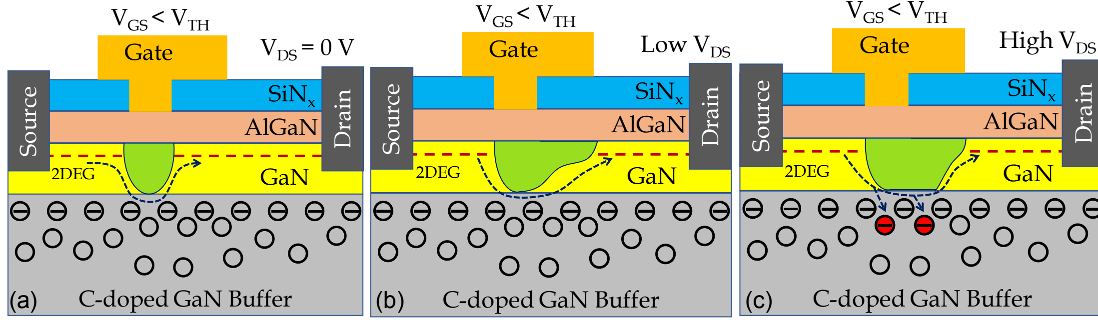

Figure 7. (a) Channel depletion by gate field pushing the leakage path deeper into GaN buffer is opposed by negatively charged acceptor ions in the carbon doped GaN buffer. (b) As the drain bias is increased while keeping the device in OFF state, the depletion region extends upto the field plate edge and the leakage current is further pushed into the carbon doped region, (c) A further increase in the drain stress enables electrons to overcome the opposing electric field by ionized acceptor ions in the GaN buffer and electrons in the leakage path get trapped in the acceptor traps present in GaN buffer.

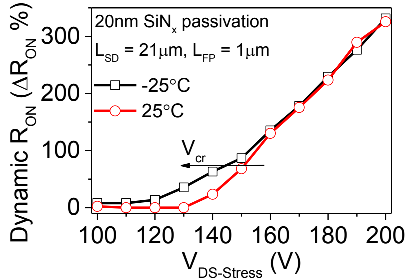

Figure 8. Dynamic R_{ON} of a device extracted at different temperatures depicts a reduction in critical voltage as temperature is reduced.

hot electrons interact with trap states in the GaN buffer giving out YL and BL signals. This phenomenon suggests presence of an opposing field preventing hot electrons from penetrating into GaN buffer till a certain threshold energy is reached. This opposing field can be explained by considering ionized acceptor traps (N_A^-) in the buffer which present a negatively charged layer in the proximity of GaN channel, resulting in an opposing force to the channel electrons (Fig. 7). Left shift in V_{cr} at lower temperature further justifies this argument (Fig. 8), as at lower temperature N_A^- will decrease and reduce the opposing electric field, lowering V_{cr}. Dependence of V_{cr} on stress time can then be explained by considering impact of source-drain (S-D) leakage on electron trapping. Trapping of electrons in the buffer traps depends on (i) number of electrons entering the carbon doped region (leakage current), (ii) area of interaction between acceptor traps and electrons (leakage path), & (iii) time period for which electrons stay there (stress time). Leakage current contours, extracted through TCAD, depict a S-D leakage path which passes through buffer underneath gate and FP (Fig. 9) and is dependent on buffer trap concentration (Figs. 9a-9c). For lower $V_{DS-Stress}$, the opposing field is strong enough to prevent channel electrons from penetrating deeper into buffer (Fig. 7a) and result in negligible DR_{ON}. As $V_{DS-Stress}$ is increased, electric field near gate and FP edge forces the leakage current to flow through the carbon doped buffer region (Fig. 7b). As enough electrons are injected into the GaN buffer, trapping of electrons takes place leading to increase in DR_{ON} (Fig. 7c). Leakage path and hence the area of interaction is then controlled by magnitude of electric field near gate and FP edge.

D. Dependence of V_{Cr} on device parameters

Based on the proposed mechanism, dependence of DR_{ON} on device parameters can be explained as follows: DR_{ON} for devices with thicker passivation layer depicts reduction in V_{cr} as L_{FP} is increased (Fig. 4). Increase in L_{FP} reduces field peak near gate edge by introducing a field peak near FP edge. Further, it increases the interaction area of leakage path with the carbon doped region as depletion region extends up to the field plate edge (Fig. 9). Thus, DR_{ON} is determined by a trade-off

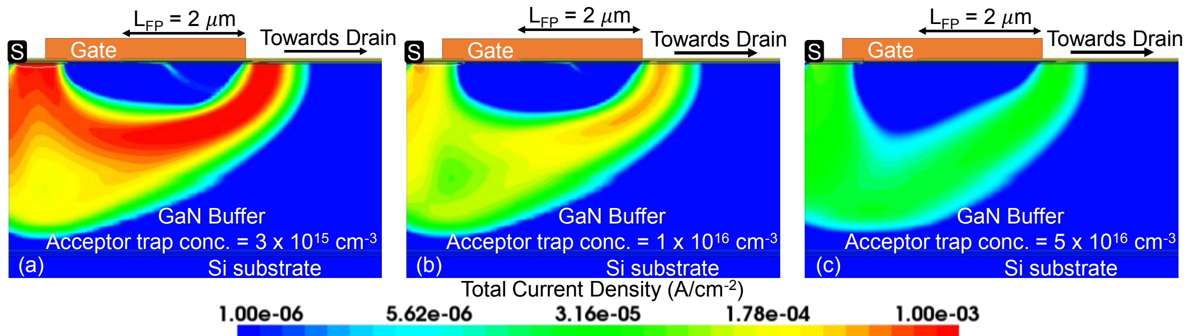

Figure 9. Current density contours extracted for a device with $L_{SD} = 15\ \mu m$ and $L_{FP} = 2\mu m$ for different acceptor trap concentrations in the GaN buffer. The contours clearly depict the leakage path to be defined by electric field at the gate and field plate edge. Further an increase in acceptor trap concentration in the GaN buffer leads to a reduction in leakage current corroborating the theory that negatively ionized acceptor ions in the buffer present an opposing field for electrons to penetrate deeper into the GaN buffer and hence lead to a lower leakage current. A $3\mu m$ buffer with undoped channel thickness of 100 nm was considered.

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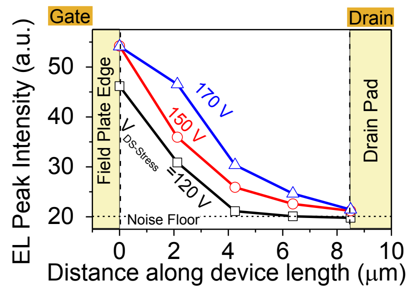

Figure 10. EL profile extracted for a similar device at different drain stress voltages. A saturation in EL intensity near field plate edge is observed as the profile extends upto the drain edge.

between field relaxation and extent of depletion region. Figs. 4(a-b) suggest that for these devices field peak near FP edge dominates DR_{ON} phenomena & hence with an increase in FP length, V_{cr} reduces and DR_{ON} increases. On the other hand, Figs. 4(c-e) depict that with increase in L_{FP}, devices with larger L_{SD} show better dynamic performance. This can be explained by comparing EL profiles for a device at different $V_{DS-Stress}$ (Fig. 10). It depicts an EL intensity peak near FP edge which is confined in a narrow region as we move away from the FP. An increase in $V_{DS-Stress}$ increases the EL intensity peak near the FP edge while the EL intensity profile now becomes broader indicating an increase in depletion width. At even higher voltages, EL intensity can be seen covering the entire drain access region and now the EL intensity peak near FP edge either reduces or remains constant. Thus, extension of depletion region up to drain edge helps in relaxing the field peak near FP edge. In this case, having a shorter L_{SD} for a shorter L_{FP} helps in reducing the DR_{ON} (Figs. 4(c-e)). However, as L_{FP} is increased beyond a critical design value, the field peak near the FP edge increases considerably leading to a significant DR_{ON} even before depletion width extends up to the drain edge, negating the advantage gained with shorter L_{SD}. As a result, devices with larger L_{FP} perform better for higher L_{SD} values. Similarly, dependence of DR_{ON} on design parameters for devices with thinner passivation layer (Fig. 4) can also be explained considering the trade-off between field peak near gate/FP edge and expansion of depletion region up to the drain contact. It is worth mentioning that with a thinner passivation layer the FP effect is more pronounced leading to higher DR_{ON} and left shift in V_{cr}.

IV. Conclusion

This work reports a critical drain stress voltage beyond which dynamic performance of GaN HEMT devices degrades significantly. Through EL, PL and temperature dependent DR_{ON} measurements it was shown that the critical voltage is not governed by generation of new traps or hot electrons but is rather defined by occupation of traps already present in the GaN buffer. Electric field at the gate/field plate edge and the opposing field applied by negatively charged ionized acceptor traps in the GaN buffer were shown to define the critical voltage. Magnitude and path of S-D leakage through the GaN buffer determined by channel depletion and channel electric field profile along with stress time were able to explain the dependence of DR_{ON} on device parameters and the observed left shift in critical voltage with increase in stress time.

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