How to Achieve Moving Current Filament in High Voltage LDMOS Devices: Physical Insights & Design Guidelines for Self-Protected Concepts

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Abstract— **New design approach for improving ESD robustness of High voltage LDMOS devices is presented using detailed 3D TCAD simulations by developing physical insights and engineering approaches for moving filaments. (i) NPN turn-on engineering by using an optimum P-well profile & substrate biasing and (ii) filament width engineering by using optimum drain diffusion length (DL), shows how static filament can be modified to achieve dynamic (moving) nature. This approach resulted in 10× improvement in ESD robustness for self-protecting concepts.**

Index Terms—Electrostatic Discharge, Laterally Double Diffused MOS (LDMOS), Current Filaments.

I. Introduction

LDMOS devices are key for building various Systems on Chips (SOC) and are used to implement high voltage functionalities in different automotive applications. In these applications, LDMOS devices can directly get exposed to ESD threats, making them vulnerable to ESD failures [1-4]. LDMOS devices in I/Os are either protected using a HV protection element like LDMOS-SCR [5], Bidirectional HV-SCR [6], which requires additional silicon footprint and add to latch up and power-scalability issues [5-6]. Dependence on external ESD protection element can be mitigated by making LDMOS self-protected by engineering the static filament into dynamic filaments. Static filament engineering pushes the onset of filamentation, while presence of dynamic filament pushes the failure limit beyond power law. In the past different works have studied filament motion using TCAD and physical interpretation of filament movement was given both in LDMOS kind of devices [7-9] and in Silicon controlled rectifier devices [10]. However, engineering dynamic filaments – particularly moving filament, and physical knobs associated with filament motion are yet not explored. This work attempts to fill this gap with a motivation to develop LDMOS design guidelines using 3D TCAD based approach, to achieve moving filaments.

II. Devices under Test & Filament Engineering Approach

Static and dynamic filaments are engineered by adjusting the LDMOS design depicted in figure 1(a). Static filament behavior is modulated through drain engineering, whereas dynamic filaments are obtained by tweaking the N-P-N action. N-P-N strength is modulated by P-well engineering (Fig. 1b). The P-well doping is used an engineering tool to modulate the P-well base resistance and hence modulate the N-P-N action. On top of P-well engineering, substrate biasing techniques is further employed to modulate the N-P-N turn on strength further. It is to mention that the practical implementation of substrate biasing during ESD strike in LDMOS/DeMOS devices was discussed

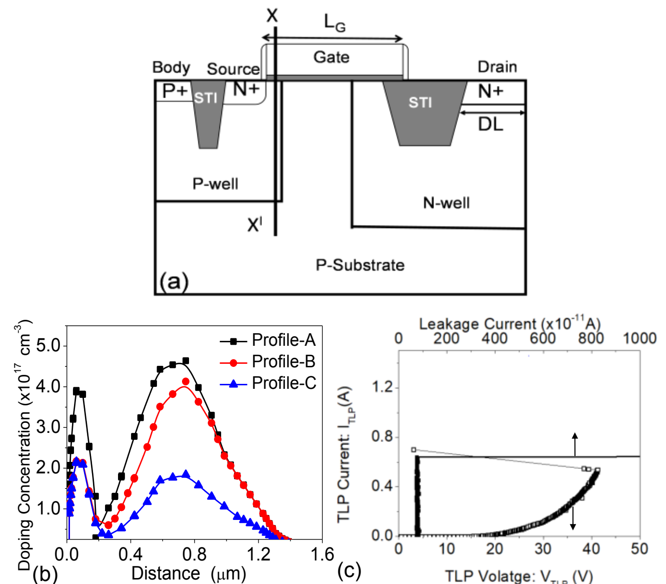

Fig. 1: (a) Cross-sectional view of high voltage LDMOS. (b) Doping profiles of different P-well in LDMOS under study. **Note:** X-axis of the plot represents the XX' line of cross-section in (a), starting from silicon surface. (c) Measured TLP I-V characteristics of typical LDMOS (PW 100ns). Inset shows the leakage current as a function stress current. Typical LDMOS devices fail at the onset of voltage snapback and provide very low ESD failure current.

Device Simulated	Doping along XX'	Substrate Biasing	DL
Type-1	Profile-A	0 V	Minimum
Type-2	Profile-B	0.4 V	Minimum
Type-3	Profile-C	0.4 V	5*Minimum

Table-1: Summary of different devices types used in this work to study the filament motion.

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and implemented in [2]. The RC trigger mechanism used to ramp gate only during ESD stress conditions, can be used to pull substrate up.

The typical LDMOS device failure at the onset of voltage snapback is measured as depicted in figure 1(d). It is worth mentioning that though the experimental data represents an LDMOS device of different voltage class, the failure is LDMOS device at the onset of voltage snapback is universally reported in most literature studies [11] unless if any engineering done to mitigate the static filament [4]. A similar failure behavior is observed in 3D TCAD simulated type-1 device, where the lattice temperature raises abruptly at the onset of voltage snapback (Fig.2). We have presented the analysis for three different types of devices in this work, particularly designed to engineer the static and dynamic

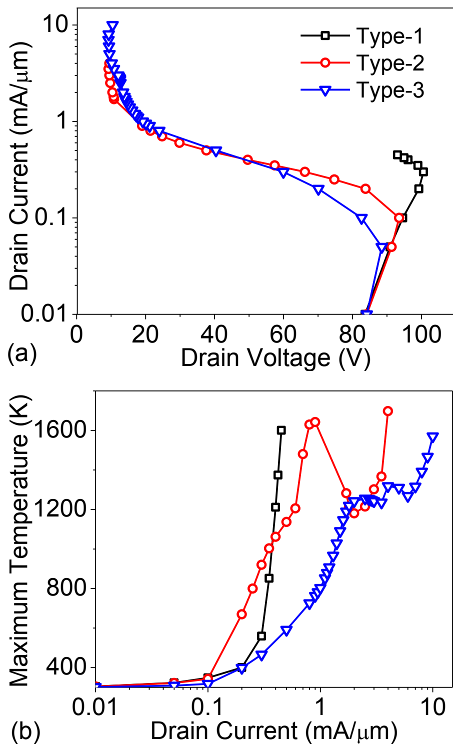

Fig. 2: (a) 3D TCAD simulated TLP I-V characteristics of different LDMOS devices under investigations (b) maximum lattice temperature plotted as a function of ITLP. Type-1 device (profile-A), fails at the onset of voltage snapback. Type-2 (Prof-B & sub biasing of 0.4V) fails in window of current during the snapback, however survives higher current. In type-3 (DL engineered with Prof-C& Vsub=0.4V) the failure current window near the snapback is eliminated and the failure current increases by 10X.

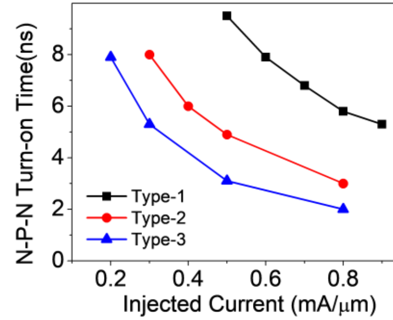

Fig. 4: N-P-N Turn on times for investigated devices. Faster N-P-N turn on, with larger DL in type-3 device yields Larger Failure current.

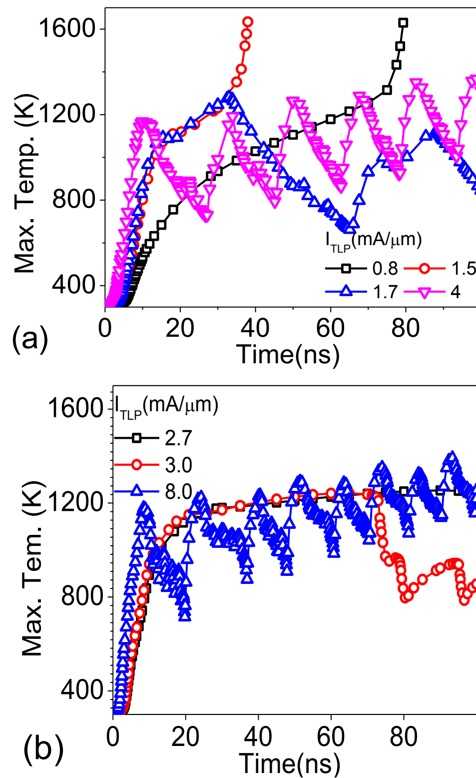

Fig. 5: The transient temperature for different injected currents. (a) Type-2 (b) Type-3 devices. The oscillations in Lattice temperature at higher injected current cause the device to survive higher currents. Failure in type-3 device at low currents is not seen attributed to DL engineering.

Filaments. Type-1 is LDMOS with P-well Profile-A, without any filament engineering techniques. This is a reference device for our investigations and as highlighted above this

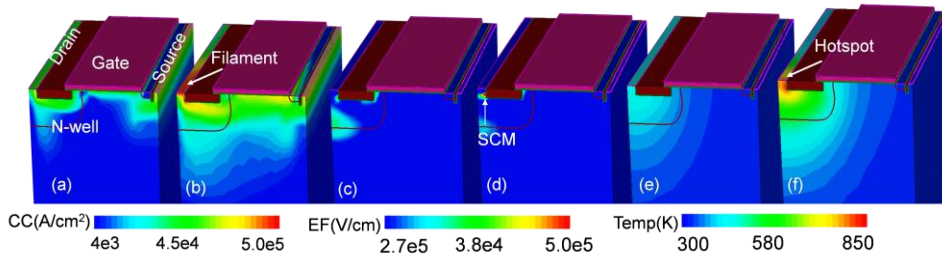

Fig. 3: Conduction current density (A/cm2)(a & b), Electric field (V/cm) (c & d), Lattice temperature (e & f)(K) in LDMOS before and at the onset of filament formation. Non uniform space charge modulation at the N+ drain contact cause filament formation and voltage snapback.

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lattice temperature, attributed to static filament formation in

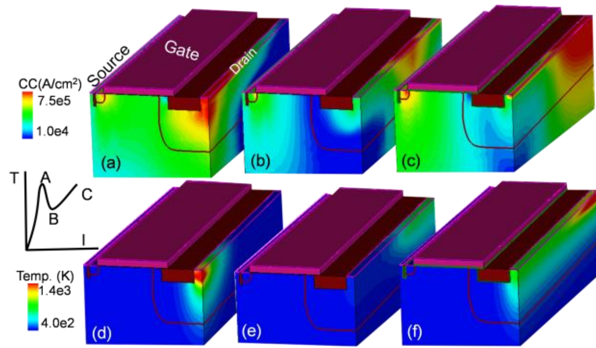

Fig. 6 Conduction current density (A/cm2)(a & b & c), Lattice temperature (d & e & f)(K) at A, B, C shown in the inset for type-2 device. At A, the static filament causes device failure, If stressed further at B, the filament motion mitigates the heating and device conducts safely until C, where it fails because of excess heating.

Device fails at the onset of voltage snapback. In type-2 device, P-well profile-B (reduced surface P-well doping) is used and substrate biasing ($V_{substrate}$) of 0.4 V is applied. The substrate potential is raised only during the ESD event. type-2 LDMOS snaps-back at lower current (It1) with lattice temperature increase until a critical temperature (Fig. 2). However, if stressed further at higher currents, lattice Temperature was found to decrease above a certain injected current (Fig. 2b). The critical temperature in this device can be as high as Si melting temperature, which makes this device vulnerable to failure in a window of currents near the snapback, while it survives high current injection levels. This unique device behavior observed in LDMOS device using 3D TCAD analysis has practical significance. The similar vulnerability of device failure in currents near snapback was experimentally demonstrated in [12]. Where it was shown that by skipping the vulnerable failure current values near the snapback region, using a low impedance load line, the device can survive the failure. However, it is worth mentioning here that the physical mechanism for device survival at higher currents in type-2 LDMOS device (in this work) are completely different from what was observed in LDMOS-SCR in [12]. The physics of device survival at higher current levels becomes clearer in the later part of this manuscript. In type-3 device, drain engineering (5 × increases in DL) is employed with P-well profile-C (reduction in surface doping), and $V_{substrate}$=0.4V applied during ESD stress. Type-3 device snaps-back at lower current than type-2, however the critical temperature was found to get reduced (Fig. 2b) below typical failure temperatures allowing device to survive the snapback or filament driven failure. This device shows a 10× improvement in It2. It is to highlight that the Increased Drain Length (DL) is not to tweak the N-P-N strength but to mitigate the static filament behavior.

III. Static Filament vs. Moving Filament Engineering

Effect of drain engineering and P-well engineering to enhance the NPN turn-on, on both static and dynamic filaments can be understood by comparing the physics of three devices types at different injected currents. Type-1 (standard reference design) device fails with abrupt raise in

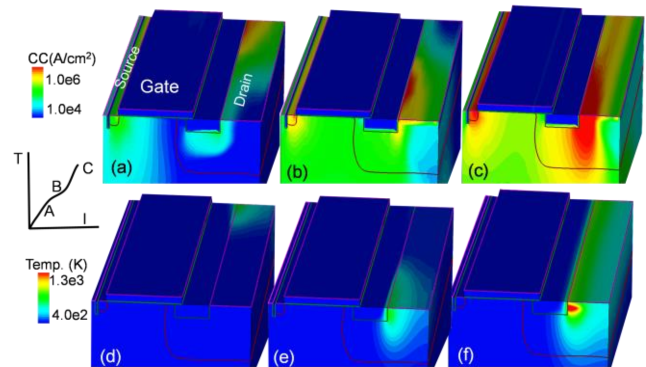

Fig. 7 Conduction current density (A/cm2) (a & b & c), Lattice temperature (d & e & f)(K) at A, B, C shown in the inset for type-3 device. Larger DL reduces the current density in the host spot region at A and device survives failure. At B Filament starts moving, and device survive till very high currents.

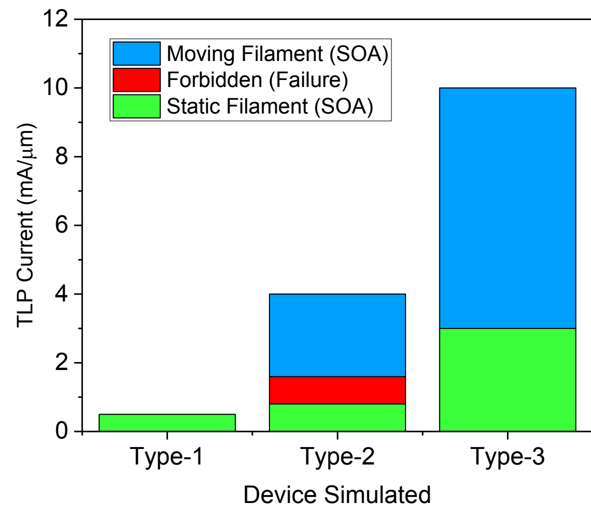

Fig. 8: Summary different device type. The type-1 device fails at the onset of voltage snapback and provides very low failure current. Type-2 device found have filament motion at higher current levels but there exists a window where the device is vulnerable for failure. However, type-3 device survives the failure window and fails at very high current attributed to filament motion. **Note:** The failure current numbers are extracted for 100 ns Pulse width.

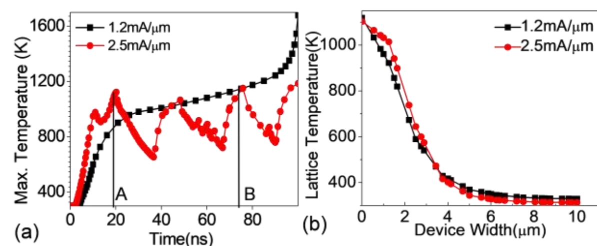

Fig. 9: (a) Transient temperature in type-2 device for two injected current. Lower current, static filament cause failure, higher current filament motion mitigates the failure. (b) The temperature plotted at two different instances of time A & B shown in (a). Larger temperature gradient causes filament motion at higher Current.

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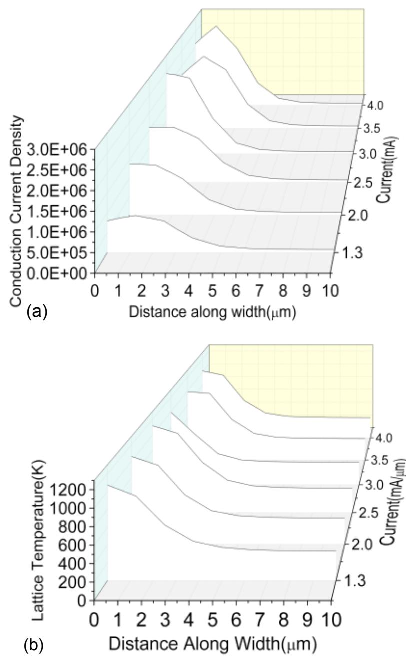

Fig. 10: (a) Conduction current density (b) Lattice temperature along device width for different injected currents, extracted at the onset of filament motion. Though the current density inside the filament is different, the temperature gradient remained similar in all the cases.

LDMOS. This is attributed to space charge modulation (SCM), which shifts the peak electric field under N+ drain region (Fig. 3d) causing mobility degradation and eventual filament formation as a balancing act [3]. Hotspot formation and failure (Fig. 3f) where the consequence of the electrical instability. Type-2 & type-3 devices attributed to higher NPN strength shows early snapback characteristics. Reduced P-well doping in type-2 & 3 devices increase P-well resistance & positive substrate biasing causes early turn-on of the source-P-well diode and deeper current conduction [2]. These attributes make NPN stronger. The enhanced N-P-N turn-on time as function of injected currents near the snapback for type-2 and type-3 devices can be seen in fig.4. The N-P-n turn-on time enhancement in Tpe-3 is not because of DL engineering but attributed to P-well engineering. After NPN turn-on, type-2 device shows early static filament formation but in type-3 device static filament is delayed to higher current levels as depicted in Fig. 5(a) & (b). This is due to reduced current density in the N-well of type-3 device (Larger DL), which pushes the onset of SCM to higher injected currents [6]. Despite SCM induced filament formation, type-3 device shows a relaxed temperature (Fig. 7) as the current density inside the hotspot is lowest for type-3 device. At higher injected currents, both type-2 and type-3 Show oscillations in lattice temperature (Fig. 5), which attributed to presence of moving current filaments (Fig. 6 & 7). Despite moving filaments, the average temperature continues to increase for all higher current levels in both type-2 and type-3 devices, which slows the filament motion and causes the device to fail eventually due to static filament.

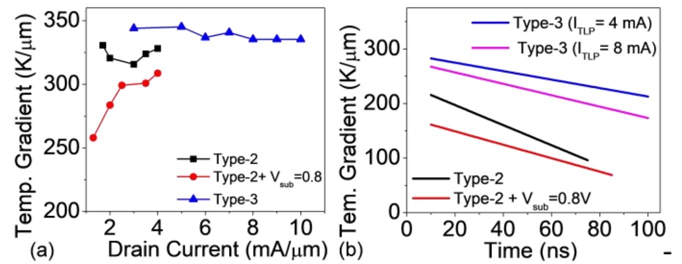

Fig. 11: (a) Temperature gradient required for filament motion as a function of injected current for different LDMOS designs under investigation (N-P-N strength). (B) Temperature gradient required for filament motion as a function of time at the same injected current but for different N-P-N strengths. Device with stronger N-P-N requires lower gradient for motion, larger DL with same N-P-N strength also requires more gradient attributed to relaxed filaments.

III. Physics of Filament Motion: New Insights

Explorations and observations so far related to NPN engineering and drain engineering brings us to the fundamental question related to the filament motion. What triggers the filament motion in LDMOS? What factors does it depend on? Transient temperature response for two current levels in type-2 device is compared (Fig. 9a). Point-A denotes the onset of filament motion at higher current, point B is where the same peak temperature is observed but for a lower current. Larger temperature gradient is observed at higher current (Fig. 9b), this is the first indication of temperature gradient as driving factor for filament to move. Further, temperature profiles plotted for different injected current, extracted at the onset of first filament motion (at different time instances for each current) in Fig .10(b) shows same temperature gradient, though the current density profiles are different (Fig. 10a). This further confirms that filament starts to move when a certain temperature gradient is reached but not at a certain current density inside the filament. It is worth mentioning here that the extracted temperature profiles in fig.10 (b) correspond to the first time instant of filament motion for that current value.

The next question to be answered regarding filament motion is, does the temperature gradient that drives filament motion a constant? Or does that vary as function of device design. It is further observed that the temperature gradient required for first filament motion, is also a function of NPN strength and thermal heat dissipation inside the device (Fig. 11). Faster NPN requires lower temperature gradient for the filament motion (Fig. 11a), however with similar NPN strength type-3 device needs larger gradient than type-2. But the temperate gradient required remains constant for different injected currents. The other fundamental question regarding the motion is does the temperature gradient required for motion increases or decreases once the filament starts moving? It is observed that, once the filament starts moving at a given injected current, the gradient require for filament motion also reduces (Fig. 11b), as the heat accumulation occur inside the device each time when filament moved through a given point. Though the filament motion is triggered by temperature gradient, the process of filament motion is explained through negative coefficient of impact

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ionization with temperature [7, 8]. When the temperature gradient reaches to its critical value inside the filament (this value is found to change as a function of N-P-N strength, heat dissipation inside the device as discussed above), the reduction in impact ionization inside the filament is higher. This meant that the impact ionization at edge of filament becomes more than the II inside the filament and hence the bipolar next to filament region turns on and the process continues as make the filament to move from one corner to other corner (Fig.12). The sensitivity of Impact ionization with the lattice temperature is shown in (Fig.13).

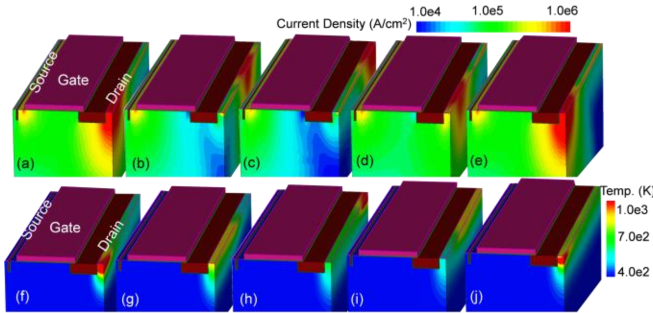

Fig. 12: (a)-(e) Current density (A/cm2) and (c)-(d) lattice temperature (K) for an injected current of (3 mA/μm). For currents beyond the observed failure window in type-2 device, moving current filaments are observed from one edge to the other edge.

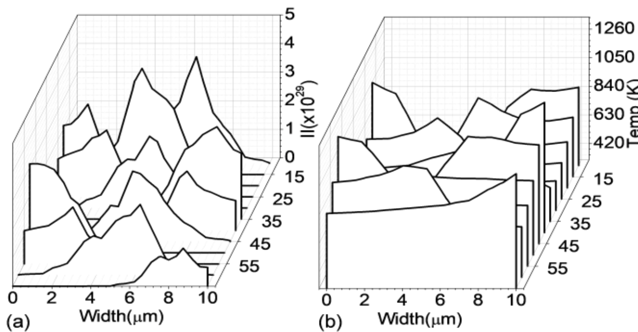

Fig. 13: (a) Impact ionization (II) (b) Lattice temperature at injected current of 3 mA/um, as a function of stress time. Negative coefficient of temperature causes the II to reduce in the filament region. This allows immediate bipolar in the width direction to conduct, hence filament moves across width until it reaches other edge, where it becomes stronger again and starts moving backwards.

IV. THE ON-STATE PERFORMANCE

The design modifications (in type-2 and type-3 devices), that are done to improve ESD robustness by tweaking the parasitic bipolar N-P-N action have found to cause very small drift in the on-state DC I-V characteristics of device, as depicted in fig.14. Out of three design changes, the P-well surface doping change will only have slight impact on the threshold voltage and hence the DC output characteristics. The substrate biasing will only raise during ESD event hence do not have influence on the functional window. DL variation even as reported in [11] do not show any influence of functional characteristics.

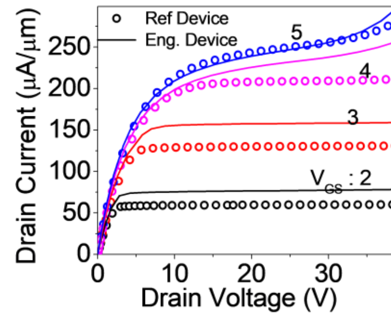

Fig. 14 Output characteristics of Standard design type-1 device along with engineered type-3 device. The engineered device yields 10X higher ESD robustness without much loos of on-state performance.

V. CONCLUSION

The temperature gradient inside the current filament is found to be the trigger point for filament motion. The gradient required for filament motion depends on NPN strength and heat dissipation inside the device. Stronger NPN need smaller gradient for filament motion. Positive substrate biasing and reduction in P-well doping, which improved the intrinsic NPN turn on, resulted in moving current filament at higher injected current. However, such LDMOS devices couldn't survive failure from static current filaments at the onset of voltage snapback. This was addressed by reducing the critical temperature during initial filament formation after voltage snapback, by using drain engineering. Drain engineering by relaxing the SCM strength lowered the current density inside the filament formed at the verge of voltage snapback. Faster NPN turn-on due to P-well and substrate bias engineering & static filament width adjustment by drain engineering provided 10× improvements in the ESD robustness. Finally, the engineered design shows negligible effect on the transistor performance.

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