Threshold Voltage Shift in a-Si:H Thin film Transistors under ESD stress Conditions

Rajat Sinha[1, 2], Prasenjit Bhattacharya[3], Sanjiv Sambandan[3, 4] and Mayank Shrivastava[1]
[1]Department of Electronic Systems Engineering, Indian Institute of Science, Bengaluru, India 560012
[2]Centre for Nano Science and Engineering, Indian Institute of Science, Bengaluru, India 560012
[3]Department of Instrumentation and Applied Physics, Indian Institute of Science, Bengaluru, India 560012
[4]Department of Engineering, University of Cambridge, Cambridge CB2 1TN, UK

Abstract— **We present physical insights into the instability behavior of hydrogenated amorphous TFTs under ESD stress using real-time current-voltage and capacitance-voltage characterization. A threshold voltage increase under moderate stress and a recovery under high stress is investigated. Impact of gate-bias and device dimension is explored. Physics of gate-bias annealing and an associated device recovery is explored. Finally, we investigate the instability behavior in a-Si:H gated diodes and explore the role of self-heating on their reliability.**

***Index Terms*—Amorphous silicon, Electrostatic Discharge, Thin film transistors, Degradation, Gated Diodes.**

I. Introduction

Hydrogenated amorphous silicon (a-Si:H) has been a subject of extensive investigations and is one of well-studied disordered materials. Thin-film transistors based on a-Si:H have formed the backbone of active matrix flat panel displays owing to their low thermal budget fabrication process and high uniformity over large areas. a-Si:H TFTs have also been used in sensing applications [1],[2], display drivers [3],[4] , solar cells [5] and light emitting diodes [6]. However, to ensure successful application of a technology, its reliable operation is necessary and thus it becomes imperative to understand the physics behind device degradation. In our earlier work, we explored physics of ESD failure of a-Si:H TFTs under ESD stress [7], a critical gap still exists in context of threshold voltage instability behavior. A thorough investigation of ESD behavior also enables explorations into the high frequency behavior and thermo-electric interactions n the device. This work aims to delve deeper into the physics of threshold voltage instability behavior of a-Si:H TFTs under ESD stress through a detailed discussion of instability mechanism under various regions of device operation and exploring how device dimensions and architecture play a role in device degradation. A detailed discussion on gate bias-anneal is undertaken to study possible recovery mechanisms and their physics. Instability mechanism in gated didoes is studied through repetitive ESD stressing.

II. Device Fabrication & Characterization

Fig.1 shows the cross-section of back channel passivated and back channel etched TFTs used in the course of this work. A piranha cleaned corning glass is used as the substrate. Gate contacts are formed through e-beam evaporation of Aluminum and Molybdenum and are then patterned using a wet etch process. Post gate-metallization, a series of plasma enhanced chemical vapor deposition (PECVD) based processes are carried out to deposit a 200 nm thick SiN_x a 150 nm thick a-Si:H layer and 300 nm thick SiN_x, where these layers serves as gate dielectric, semiconductor channel and top passivation respectively. Following the patterning of passivation layer, a 30nm thick n-doped a-Si:H layer was deposited using PECVD. Reactive ion etching (RIE) was employed to etch-out the n-doped a-Si:H layer from the channel region. Subsequently, the active layer and the gate insulator were patterned using RIE. The source/drain electrodes, composed of Aluminum and Molybdenum were deposited using DC sputtering and patterned by wet etch. The devices were annealed at 423K for a period of 1hr before characterization. ESD characterization was done using a 50 Ω TLP setup [8]. A pulse generator with the capability to apply voltage levels up to 2 kV is used. A current sensor with a sensitivity of 0.5 mV/mA and a 4 GHz digital phosphor oscilloscope are used to capture voltage and current waveforms. The resultant waveforms are averaged in a pre-determined averaging window (here, 60-80 % of pulse width) and the extracted

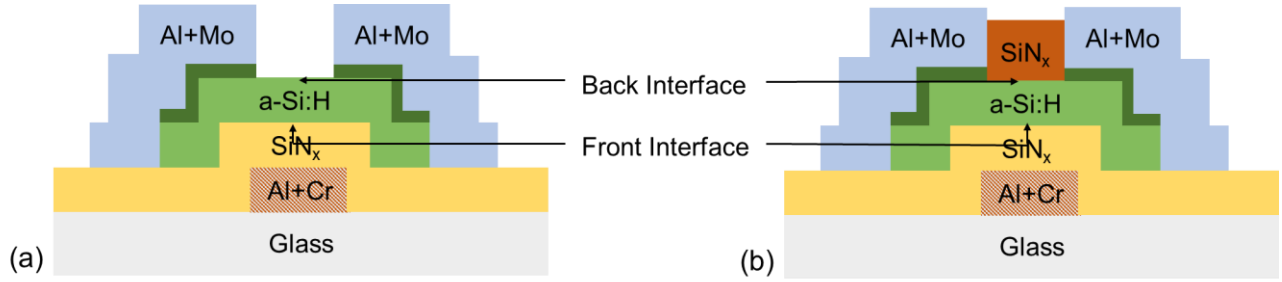

Fig.1: Cross-sectional view of (a) Back Channel Etched (b) Back Channel Passivated TFT used in this work.

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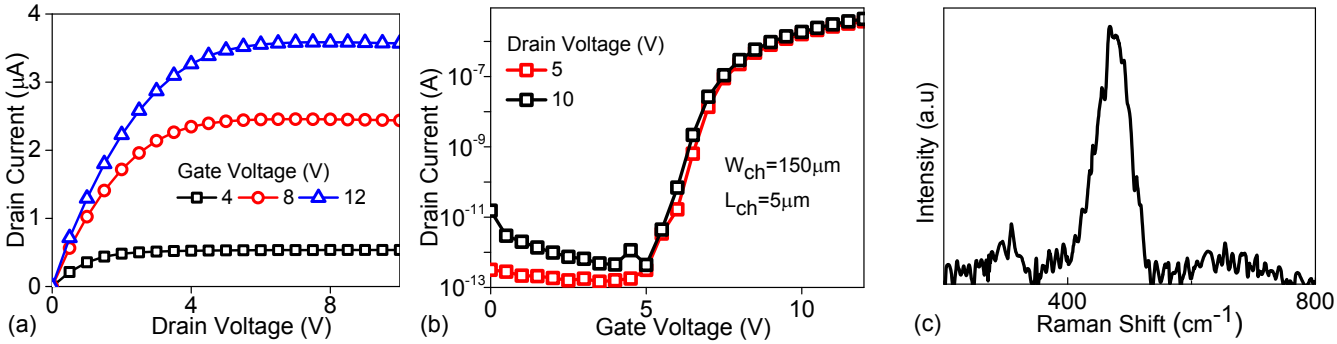

Fig. 2: DC (a) Output (b) Transfer characteristics of a a-Si:H TFTs and (b) Raman spectra of a-Si:H.

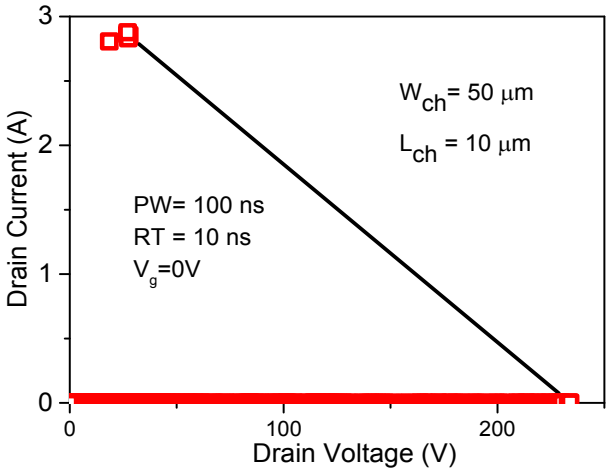

Fig 3: TLP characteristics of a typical a-Si:H TFT.

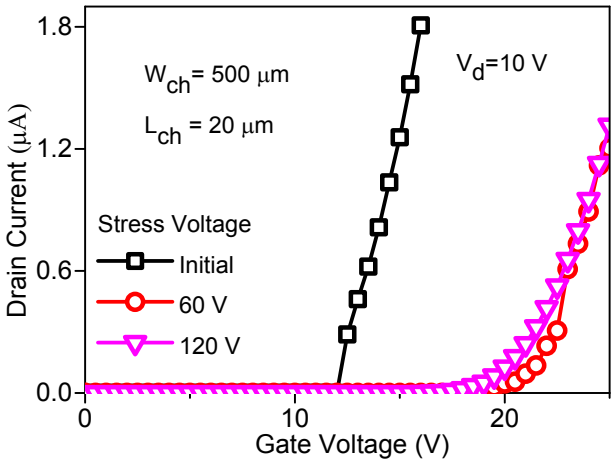

Fig 4: DC characteristics of a-Si:H TFT under floating gate ESD stress condition.

current, voltage values are used to plot a quasi-static I-V characteristics of the device. The setup is calibrated using a standard surface mount resistor and a Zener diode. Unless stated otherwise, a pulse, of time period 100ns and rise time 10ns. Exploration of device degradation is done by on-the-fly current-voltage and capacitance-voltage measurements post application of pre-determined stress voltage levels. Fig. 2 shows DC I-V characteristics of devices under test along with a Raman signature of a-Si:H (Fig. 2c). Fig. 3 shows the typical TLP characteristics of a a-Si:H TFT under grounded gate ESD stress condition. It can be observed that the device current under ESD conditions is much smaller than the least count of the setup (in this case 50 μA).

III. RESULTS AND DISCUSSIONS

Fig. 4 and 5 show the DC I-V and C-V characteristics of a-Si:H TFT stressed in floating gate condition. The devices are stressed under ESD conditions with a pulse width of 100 ns and a rise time of 10 ns. It can be observed (Fig. 4) that as stress initially increases, threshold voltage (V_T) increases. However, on further increasing the stress, there is a recovery in V_T. It can also be observed that as stress is initially applied, C-V characteristics present a parallel shift from the initial conditions (Fig. 5a). As the stress is further increased, C-V present a stretched out behavior compared to the initial C-V characteristic. This can be explained as follows: As stress is

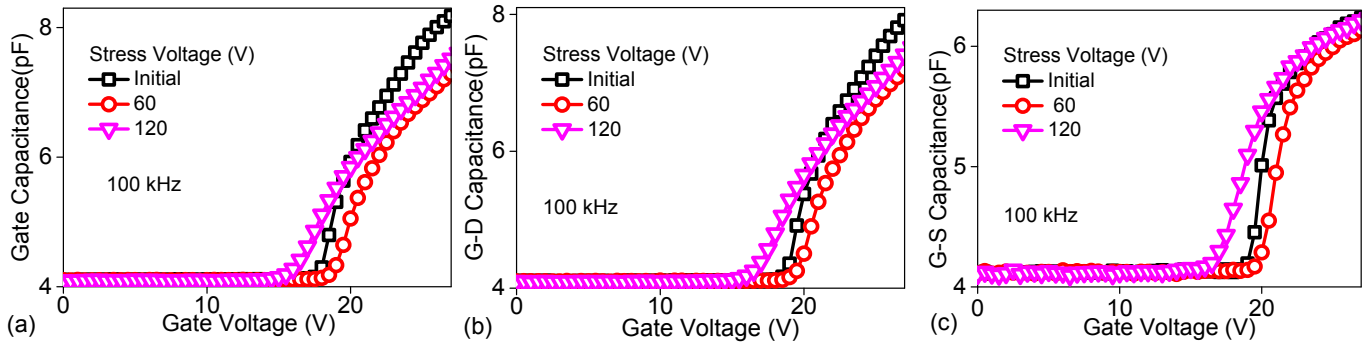

Fig.5: C-V characteristics of a-Si:H TFT under floating gate ESD stress condition.

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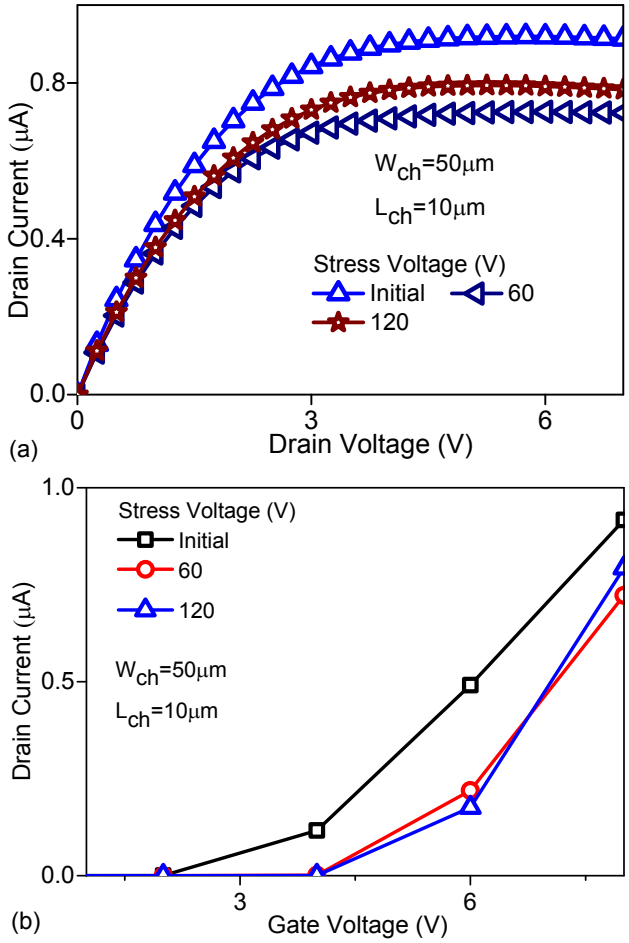

Fig.6: DC I-V characteristics of a-Si:H TFT stressed under grounded gate ESD condition.

initially applied, there is electron trapping in dielectric, which leads to V_T increase. Further increasing the stress, positively charged defect creation in the channel takes place and V_T recovers [9]. The creation of positively charged defect states can be inferred from a negative shift in C-V characteristic at high stress levels. As the electric field across the a-Si:H channel increases, electrons gain enough energy and collide with a-Si network leading to defect creation. It can also be observed from Fig. 5b and 5c, that the stretched out behavior of C-V characteristics is present in both gate-drain and gate-source capacitance, however the extent of defect creation is higher on the drain side of the channel. This behavior points to the fact that defect creation takes place near both the contacts but is spatially non-uniform in its extent. This can be explained as follows: The fermi level in the gated region during floating condition is ambiguous and fermi level shift near both drain and source would lead to field concentration in the region, leading to defect creation although the scale of defect creation may not be uniform across the channel.

Fig. 6 shows the DC I-V characteristics of a-Si:H TFT stressed under grounded gate conditions under similar pulse parameters as that of floating gate stress. The device presents a similar V_T recovery behavior under high stress conditions and is consistent with findings of an earlier study [7].

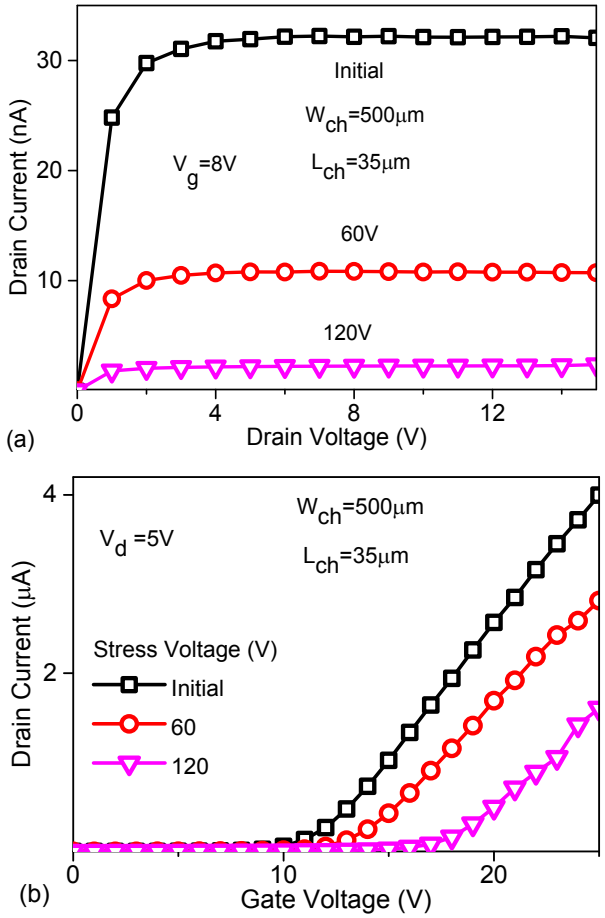

Fig.7: DC I-V characteristics of a-Si:H TFT with a larger channel length

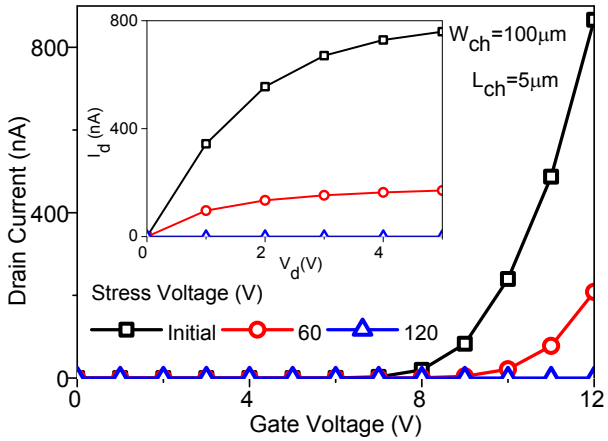

Fig.8: DC I-V characteristics of a-Si:H TFT stressed under inversion region.

The impact of device dimensions on the instability behavior is explored by varying the device channel length. As the channel length of the device is increased, the V_T recovery does not take place (Fig. 7). This behavior is attributed to dominance of electron trapping at high stress levels over defect creation, due to lower electric field in the channel. Further exploration of device degradation is undertaken by stressing the device in inversion region of operation. This is

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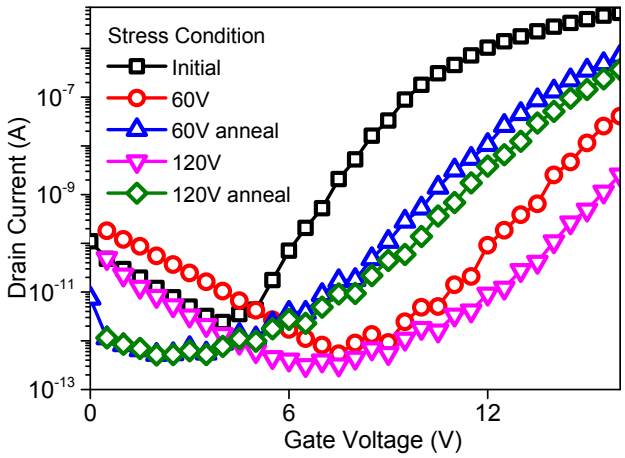


Fig.9: I_d-V_g characteristics of TFT for different steps in the characterization sequence showing the impact of gate bias anneal.

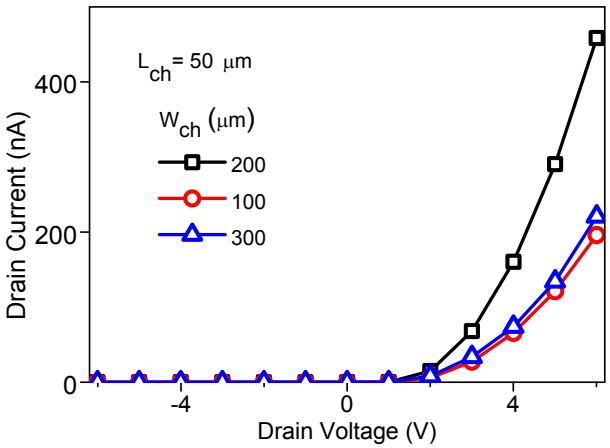
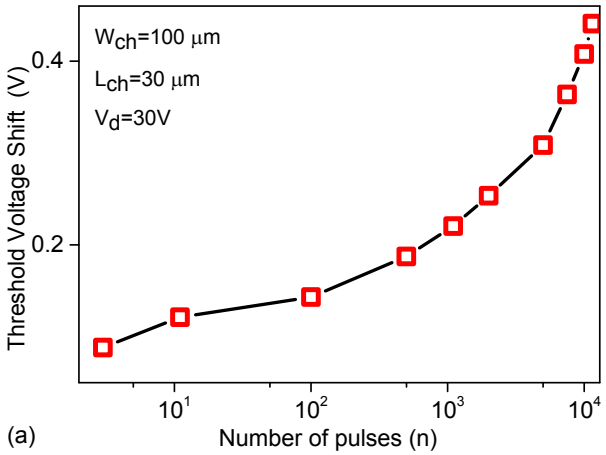


Fig 10: DC I-V characteristics of diode-connected TFTs.



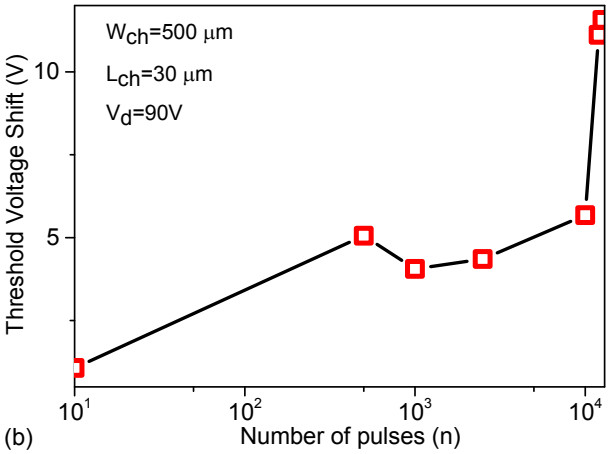


Fig.11: V_T shift of gated diode with number of pulses for repeated stressing at various stress levels.

achieved by biasing the gate at -6V while the ESD stress is applied to the device. It can be observed from fig. 8 that the device under inversion does not present V_T recovery behavior at high stress level. This can be explained as follows: In the inversion region of operation, the fermi level in the gated region is shifted down and thus peak electric field in the gate-drain overlap is reduced. Inversion operation also reduces the concentration of charge carriers in the channel. This reduction in the peak electric field coupled with reduced charge carrier concentration leads to reduced defect creation. This leads to a monotonous increase in V_T at different stress levels due to dominance of electron trapping.

1) Influence of gate bias-anneal

To further understand the physics of threshold voltage shift in a-Si:H TFTs, influence of gate bias-anneal on V_T recovery is explored. The impact of gate bias-anneal is explored by using the following characterization sequence: The DC I-V characteristics of an unstressed device is measured (Fig.9) and is followed by stressing the device to a pre-determined stress level. Post stressing, the device I-V characteristics are measured again to evaluate the degradation behavior. This step is followed by annealing the device through application of a gate bias of -10V for a period of 1200 seconds and the V_T shift is again evaluated through DC I-V measurements. The device is then stressed to a higher level and DC characteristics are measured and then a gate bias-anneal is performed and DC characteristics are measured. Fig. 10 shows the I_d-V_g characteristics of a-Si:H TFT and presents the impact of gate bias-annealing on the device performance. It can be observed that V_T recovers due to gate-bias annealing. This behavior can be explained either through trapping of hole in the dielectric or de-trapping of electrons, which were trapped earlier in the dielectric, due to applied gate bias. These mechanisms leads to an observed V_T recovery on the application of gate bias.

2) Instability behavior under simultaneous gate-drain stress

Further exploration of threshold voltage shift in a-Si:H TFTs is performed by stressing the drain and the gate contacts simultaneously. This characterization is undertaken by connecting the TFTs in a diode configuration (gated diode) and stressing the gate contact. These investigations also leverage the exploration of instability behavior in a-Si:H gate diodes, which have potential applications in switching [10],

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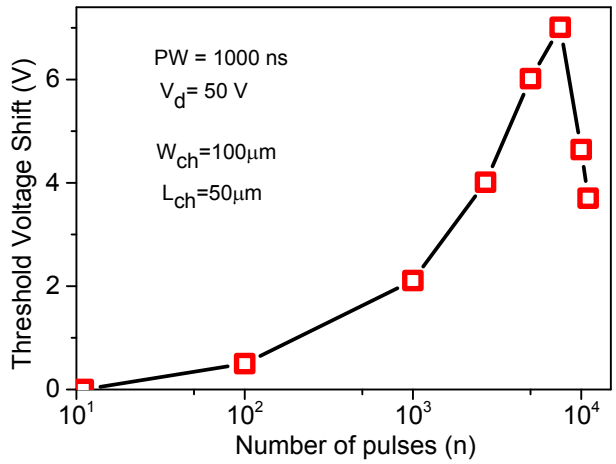

Fig. 12: V_T shift of gated diode with higher channel length with number of pulses.

voltage amplifiers [11] and V_T compensation circuits [12]. Fig. 10 shows the DC I-V characteristics of a typical a-Si:H gated diodes. The instability behavior in gated diodes is explored by stressing the device at a pre-determined stress level repetitively and measuring the V_T of the device after a certain number of pulses. It should also be noted that V_T in gated diodes is taken to be the voltage level at which the device current reaches 1nA. Fig. 11 presents the variation of V_T with number of pulses (and thus time) at various stress levels. It can be observed from Fig. 11a and Fig. 11b that the V_T shift follows a power law behavior of the form $A+n^B$ with the number of stress pulses. This behavior is indicative of defect creation lead instability in the a-Si:H channel [13]. It is also worth noting that the value of B in above equation is a function of temperature for a-Si:H and is found to be similar for the case of both low and high stress level (Fig.11), indicating that the instability behavior is electrical in nature and self-heating does not play a dominating role in device degradation. To further explore the instability behavior in gated diodes, devices are stressed with higher pulse duration (pulse width of 1000 ns and rise time of 10ns) stressed under similar low field condition. Fig. 12 presents the variation of V_T with number of pulses. It can be observed that initially, the V_T shift follows a power law behavior with the number of pulses. This behavior is similar to what is observed for device with smaller pulse duration and is indicative of defect creation as a dominant instability mechanism. Further application of stress pulse leads to a logarithmic relation between V_T shift and number of pulses. This implies that continued application of stress leads to domination of electron trapping in the dielectric as the instability mechanism [13]. This behavior can be explained though thermal excitation of charge carriers into the dielectric as a result of device self-heating.

IV. Conclusions

In this work, we have investigated the instability behavior of a-Si:H TFTs under ESD stress conditions. Physics of device degradation under ESD stress is studied through a case study of floating gate stress. It is revealed that electron trapping in the dielectric dominates the instability behavior at lower stress levels. At higher stress levels, positively charged defect creation is found to dominate the instability behavior. It is also found that defect creation takes place near both source and drain contacts, however a higher extent of defect creation takes place near the drain contact. ESD stress under grounded gate is studied and a similar instability behavior involving V_T recovery at high stress levels is reported. The impact of device dimensions on the instability mechanism is studied and it is observed that as the channel length of the device increases, electron trapping dominates even at higher stress levels. The instability behavior under inversion region of operation is studied and it is observed that in inversion operation, V_T recovery does not take place and electron trapping in dielectric dominated the device degradation. The influence of gate bias-anneal is studied and is found to improve device behavior by enhancing hole trapping in the dielectric or through de-trapping the electrons from the dielectric. Finally, instability behavior under simultaneous gate-drain stress is studied and is found to be defect creation dominated even under low stress levels. Self-heating shows little to no impact at high stress levels at low pulse widths. Upon increasing the pulse width in gated diodes, self-heating presents itself through thermal excitation of charge carriers into the dielectric at longer stress duration.

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