Analysis of Energy Quantization Effects on Single-Electron Transistor Circuits

Surya Shankar Dan and Santanu Mahapatra, *Member, IEEE*

***Abstract*—In this paper, the effects of energy quantization on different single-electron transistor (SET) circuits (logic inverter, current-biased circuits, and hybrid MOS-SET circuits) are analyzed through analytical modeling and Monte Carlo simulations. It is shown that energy quantization mainly increases the Coulomb blockade area and Coulomb blockade oscillation periodicity, and thus, affects the SET circuit performance. A new model for the noise margin of the SET inverter is proposed, which includes the energy quantization effects. Using the noise margin as a metric, the robustness of the SET inverter is studied against the effects of energy quantization. An analytical expression is developed, which explicitly defines the maximum energy quantization (termed as "*quantization threshold*") that an SET inverter can withstand before its noise margin falls below a specified tolerance level. The effects of energy quantization are further studied for the current-biased negative differential resistance (NDR) circuit and hybrid SETMOS circuit. A new model for the conductance of NDR characteristics is also formulated that explains the energy quantization effects.**

***Index Terms*—Coulomb blockade, energy quantization, Monte Carlo (MC) simulation, noise margin, orthodox theory, single-electron transistor (SET).**

I. Introduction

IN THE RECENT past, the hybridization of single-electron transistor (SET) with CMOS technology has attracted much attention [1], [2]. Such integration can offer new functionalities, which are very difficult to achieve either by pure CMOS or by pure SET approaches. As a result, silicon SETs are appearing to be more promising than metallic SETs for their possible integration with CMOS. SETs are normally studied on the basis of the classical orthodox theory [3], where quantization of energy states in the island is completely ignored. Though this assumption greatly simplifies the physics involved, it is valid only when the SET is made of metallic island. As one cannot neglect the energy quantization in a semiconductive island, it is extremely important to study the effects of energy quantization on silicon SET logic performance.

In this paper, primarily, the effects of energy quantization on voltage-state SET inverter performance are analyzed using Monte Carlo (MC) simulation and analytical modeling. It is found that energy quantization mainly alters the Coulomb blockade region and the drain current of SET devices, and thereby, it affects the noise margin, power dissipation, and the propagation delay of the SET inverter. A new model is proposed for the noise margin of the SET inverter by including the energy quantization effects. Using the noise margin as a metric, the robustness of the SET inverter is studied against energy quantization. It is found that the SET inverter designed with $C_T : C_G = 0.366$ (where C_T and C_G are tunnel junction and gate capacitances, respectively) offers maximum robustness against the energy quantization.

The study is further continued for current-biased SET (CBS), which is an integral part of almost all hybrid CMOS-SET architectures [1], [2] as it provides unique triangular periodic output with monotonous increase of its gate voltage. It is found that energy quantization has no impact on the gain of the CBS characteristics though it changes the output voltage levels. The effects of energy quantization are then studied for two CBS-based SET circuits: one is pure SET-based negative differential resistance (NDR) [4], [5] and the other is hybrid CMOS-SET-based SETMOS [6] cell.

The energy quantization effects start to appear in SET characteristics when the dimension of the SET island becomes comparable to the Fermi wavelength of the electrons, which is inversely proportional to the free electron density. Therefore, the amount of energy quantization in the SET island depends on several properties of the island like size, shape, material, doping concentration, property of the tunnel barrier, etc. In this paper, we have not attempted to deal with the complex quantum physics involved in obtaining a definite value of energy gap between two successive energy levels (ΔE) for any particular device geometry. Here, ΔE is treated as an *electrical parameter* so that we can study the effects of energy quantization when it is *gradually* introduced into a metallic island without detailing how to obtain the exact value of ΔE for the structure. The problem of developing analytical expressions for the quantum physics involved in ΔE itself is a complicated work and is *not* the objective of this paper. However, the range of values considered in all our simulations as well as our development of the analytical model are quite practical, as they are in the range of quantized energy steps analogous to square potential well problem (if we consider energy quantization is solely due to the island geometry), which are often encountered in low-dimensional physics. It should be noted that, here, we use parabolic potential well so that all ΔE's are equal to avoid complication.

II. Modeling and Simulation Methodology

In this paper, the widely accepted single-electron device simulator SIMON [7] is used to comprehend the effects of

Manuscript received January 20, 2009; revised April 24, 2009. Current version published January 8, 2010. This work was supported by the Council of Scientific and Industrial Research (CSIR), India, under Grant 22 (0453)/07/EMR II. The review of this paper was arranged by Associate Editor M. P. Anantram.

The authors are with the Nano-Scale Device Research Laboratory, Centre for Electronics Design and Technology, Indian Institute of Science, Bengaluru 560012, India (e-mail: dsurya@cedt.iisc.ernet.in; santanu@cedt.iisc.ernet.in).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNANO.2009.2022833

Authorized licensed use limited to: INDIAN INSTITUTE OF SCIENCE. Downloaded on January 13, 2010 at 00:50 from IEEE Xplore. Restrictions apply.

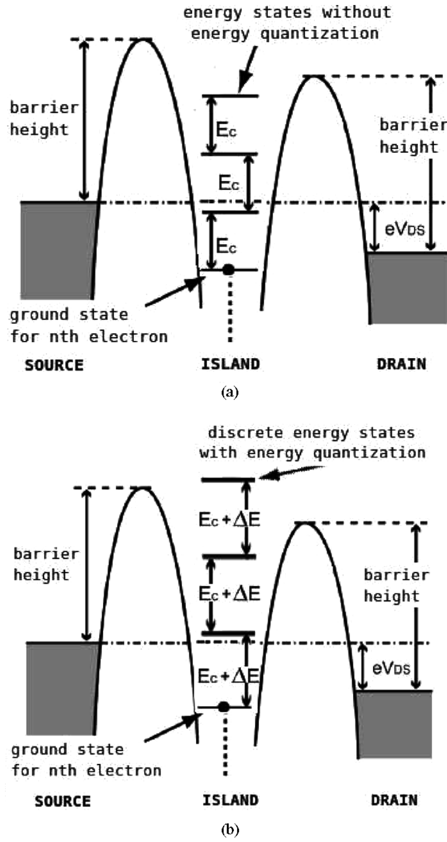

Fig. 1. Schematic of the energy diagram of an SET (a) with and (b) without energy quantization. Here, E_c is the charging/addition energy. (adapted after [11]).

energy quantization. So far, SIMON has been used extensively to study circuits based on metallic SET having continuous energy states. Simulating single-electron tunneling in SETs with islands having discrete energy levels is not so straightforward like simulating a metallic SET. Because of this reason, to our best knowledge, SIMON has never been used to study the effect of energy quantization on the SET circuit. In this paper, for the first time, we have demonstrated how to use SIMON in order to study such the effects by gradually introducing energy quantization in a metallic SET. Fig. 1 shows the situation inside the island with (a) continuous energy states (as in metals) and (b) discrete energy states (as in semiconductors). The total tunnel rate (Γ) from the occupied states (initial states i) on one side of the barrier to the unoccupied states (final states f) of the other side of the barrier, considering the change in free energy and using Fermi's golden rule, can be expressed as the following summation [8], [9]:

$$\Gamma(\Delta G) = \frac{2\pi}{\hbar}|T|^2 \int_{E_{c,i}}^{\infty} \int_{E_{c,f}}^{\infty} D_i(E_i) D_f(E_f) f(E_i) \times\{1 - f(E_f)\}\delta(E_i - E_f - \Delta G) dE_f dE_i \quad (1)$$

where $f(E)$ is the Fermi–Dirac distribution, T is the transmission probability, $E_{c,i}$ ($E_{c,f}$) is the conduction band edge of the side where electron resides initially, i.e., initial side (tunneling to final side), and $D_i(E_i)$ and $D_f(E_f)$ are the densities of states (DOSs) on the initial and final sides of the barrier. For metallic islands, the DOSs D_i and D_f may be considered as constant in the small window of energy $f(E_i)\{1 - f(E_f)\}$ and can be taken out of the integral. Thus, (1) reduces to the orthodox theory expression for single-electron tunneling rate, which is given by

$$\Gamma(\Delta G) = \frac{\Delta G}{q^2 R_T \{1 - \exp(-\Delta G/k_B T)\}} \quad (2)$$

where ΔG denotes the change in Gibbs free energy of the electron during tunneling, q, k_B, and T denote the elementary charge, Boltzmann constant, and the temperature (in kelvin), respectively, and $R_T = \hbar/2\pi q^2 |T_{if}|^2 D_i D_f$ denotes the phenomenological quantity called "*tunneling resistance*." In SIMON, R_T has to be specified by the user.

For nonmetallic islands with discrete energy levels, in order to calculate the total tunneling rate, one typically starts from Fermi's golden rule as mentioned before. The only difference is that now we cannot take $D_f(E_f)$ as a constant since the DOS for a discrete energy spectrum is a sum of delta functions. A more realistic treatment would be to consider finite lifetime broadening that introduces the Lorentzian shape functions instead of the delta functions, which is given as [9], [10]

$$D_f(E_f) = \frac{\hbar}{2\pi} \sum_n \frac{\gamma}{(E_n - E)^2 + (\hbar\gamma/2)^2} \quad (3)$$

where E_n are the discrete energy levels (due to quantization) in the island, and γ denotes the *total exit* rate in inverse second from any particular energy state, which determines the shape of the Lorentzian function. For $\gamma \to 0$, the Lorentzian approaches an ideal delta function. Using this formulation, deriving the tunneling rate expression from first principles (as followed in the orthodox theory) for the realistic case of infinite number of energy states leads to the same expression (2), with the tunneling resistance term changing into

$$R'_T = \frac{R_T}{[(\hbar\gamma/2\pi D_f)/((E_n - E)^2 + (\hbar\gamma/2)^2)]}. \quad (4)$$

The height $H = (\hbar\gamma/2\pi D_f)$ and width $W = (\hbar\gamma/2)$ used in SIMON, which define the Lorentzian shape, are constants related to the total exit rate from any particular energy state (γ) [8]–[10] and need to be tuned manually, as discussed in the following section.

One might conceptualize a metallic SET to be equivalent to a nonmetallic one in which the energy states of the island extend from lower bound $E_{\min} \to -\infty$ to upper bound $E_{\max} \to +\infty$ with the energy gaps between successive energy states $\Delta E \to 0$. In order to study the energy quantization effects, we first simulate an SET with metallic (continuous energy spectrum) island for a particular set of device parameters (C_G and C_T are given in units of attofarad and R_T is given in units of megaohm, where C_G is the gate capacitance, C_T is the tunnel junction capacitance, and R_T is the tunnel junction resistance). Then, for the same set of device parameters, we simulate a nonmetallic SET with discrete states, where $E_{\min} = -1$ eV, $E_{\max} = 1$ eV, and $\Delta E = 0.01$ meV. As the magnitudes of $E_{\min}$ and $E_{\max}$ are much larger and ΔE is much

Authorized licensed use limited to: INDIAN INSTITUTE OF SCIENCE. Downloaded on January 13, 2010 at 00:50 from IEEE Xplore. Restrictions apply.

smaller than the charging energy (tens to hundreds of millielectronvolts) of the SET, we can expect that such a device should behave as metallic SET if W and H parameters are properly tuned. After exhaustive simulations, we have found that for $H = 0.04$ eV^2 and $W = 0.001$ eV, the I–V characteristics of the nonmetallic SET with discrete energy states completely superimposes over the characteristics obtained from the metallic SET having the device parameters $C_G = 2$ aF, $C_T = 1$ aF, and $R_T = 1$ MΩ (for $C_\Sigma = C_G + 2C_T = 4$ aF, where C_Σ denotes the net capacitance at the island with respect to the ground). For a smaller device with $C_G = 0.5$ aF, $C_T = 0.25$ aF (i.e., $C_\Sigma = 1$ aF), and $R_T = 1$ MΩ, the H and W parameters were found to be $H = 0.01$ eV^2 and $W = 0.001$ eV. It is further observed that these values of H and W are almost independent of device capacitances within 50% change in the magnitudes of the device parameters. Using these calibrated magnitudes of H and W, keeping $E_{\max}$ and $E_{\min}$ constant, the value of ΔE has been gradually increased in order to simulate the effects of energy quantization on SET device and circuit performances.

When energy quantization is introduced, the net change in electron energy (ΔF) during tunneling becomes the sum of electrostatic energy contributed by Gibbs free energy (addition energy) and the energy gaps between the quantized energy levels (excitation energy). Consequently, including the quantization term ΔE into the expression for the net energy change ΔF for $n \to n + 1$ transition, we obtain [11]

$$\begin{Bmatrix} \Delta F_{s,i} \\ -\Delta F_{i,s} \end{Bmatrix} = \frac{q}{C_\Sigma}\left[C_T V_{DS} + C_G V_{GS} - nq \mp \frac{q}{2}\right] - \begin{Bmatrix} (n+1) \\ n \end{Bmatrix} \Delta E \quad (5)$$

$$\begin{Bmatrix} \Delta F_{i,d} \\ -\Delta F_{d,i} \end{Bmatrix} = \frac{q}{C_\Sigma}\left[(C_G + C_T)V_{DS} - C_G V_{GS} + nq \mp \frac{q}{2}\right] - \begin{Bmatrix} n \\ (n+1) \end{Bmatrix} .\Delta E \quad (6)$$

In (5) and (6), the upper term in the left-hand side equates the upper symbol sequence on the right-hand side and *vice versa* for the lower term in the left-hand side. For the sake of compactness throughout the paper, we have coupled two equations into one in the same manner. Here, C_Σ is the total island capacitance with respect to the ground (equal to $C_G + 2C_T$), and n denotes the number of electrons in the island and $\Delta F_{\text{initial,final}}$ denotes the net free energy change for the electron tunneling from "*initial*" to "*final*," which may be any of the source "s," island "i," or drain "d" region.

Therefore, one might approach the energy quantization problem in two ways: one is the way SIMON handles it by replacing D_f in the orthodox model with its discrete equivalent, which is given in (3), and keeping the net energy change term (ΔF) in (5) and (6) equal to the Gibbs free energy change ΔG, excluding the energy quantization term involving ΔE. The other approach, which is more elegant for developing the compact model, is to consider energy quantization as an additive term to the Gibbs free energy resulting in the expressions for *net* energy change ΔF as given in (5) and (6), and keeping the D_f term constant as in the orthodox theory. This approach is accurate when the energy gaps between successive energy levels inside the island are extremely small compared to the electron charging energy q^2/C_Σ, and there are (practically) infinite number of energy levels in the island. This situation is quite realistic in case of semiconductor islands where the quantized energy gaps between the adjacent energy levels are few orders of magnitude lower than the charging energy at practically realizable SET dimensions. The later approach is used in this paper to develop analytical models for SET circuits, and it gives good agreement with SIMON simulation.

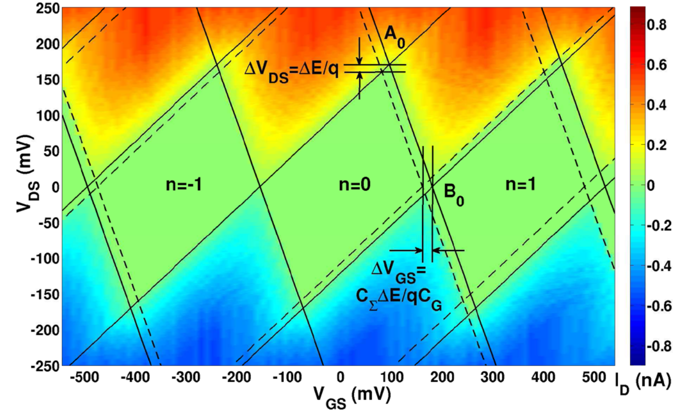

Fig. 2. Influence of energy quantization on $V_{DS} - V_{GS}$ surface characteristics (drain current contour) of an SET. The solid and broken lines represent the solution of $\Delta F = 0$ for quantized ($\Delta E = 10$ meV) and continuous ($\Delta E = 0$) energy levels in the island, respectively. (simulated for $R_T = 1$ MΩ, $C_G = 0.5$ aF, $C_T = 0.25$ aF, and temperature $T < q^2/k_B C_\Sigma = 90$ K).

III. Result and Discussion

A. Energy Quantization Effects on SET Device

Fig. 2 shows the $V_{DS} - V_{GS}$ surface characteristics (drain current contour) as obtained from the SIMON simulation for $\Delta E = 10$ meV, and the four linear equations represented by (5) and (6) are plotted with $\Delta F = 0$ for different n, and they encompass the four sides of the so-called "Coulomb blockade parallelogram." It is evident from Fig. 2 that energy quantization increases the area of the Coulomb blockade as indicated by the region enclosed by the solid lines being more than that of the broken lines. By solving these four linear equations, the coordinates of the intersection points A_n and B_n (see Fig. 2) are found to be

$$A_n \equiv \left[\frac{nq}{C_G} + \frac{q}{2C_\Sigma} + \frac{\Delta E}{q}\left(n + \frac{C_G + C_T}{C_G}\right), \frac{q}{C_\Sigma} + \frac{\Delta E}{q}\right] \quad (7)$$

$$B_n \equiv \left[(n-1)\frac{q}{C_G} + n\frac{\Delta E}{q}, 0\right]. \quad (8)$$

Using (7) and (8), the increase of Coulomb blockade area due to energy quantization could be found as

$$\Delta\text{area} = \frac{\Delta E}{q}\left[q\left(\frac{1}{C_G} + \frac{1}{C_\Sigma}\right) + \frac{\Delta E}{q}\right]. \quad (9)$$

Authorized licensed use limited to: INDIAN INSTITUTE OF SCIENCE. Downloaded on January 13, 2010 at 00:50 from IEEE Xplore. Restrictions apply.

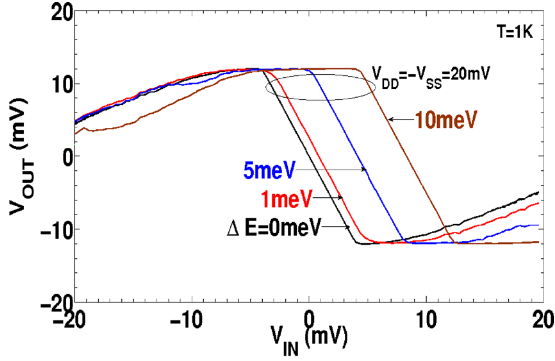

Fig. 3. Influence of energy quantization ΔE on $V_{\rm OUT}$ versus $V_{\rm IN}$ characteristics at constant $V_{DD} = -V_{SS} = 20$ mV plotted for capacitance ratio $\alpha = C_T/C_G = 1/3$ (simulated for $R_T = 1$ MΩ and $C_G + C_T = 4$ aF).

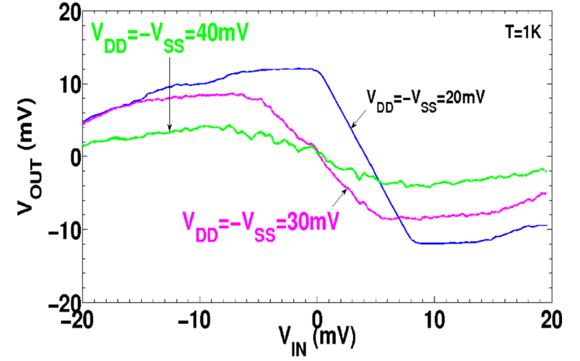

Fig. 4. Influence of bias V_{DD} $(= -V_{SS})$ on $V_{\rm OUT}$ versus $V_{\rm IN}$ characteristics at constant $\Delta E = 5$ meV plotted for capacitance ratio $\alpha = C_T/C_G = 1/3$ (simulated for $R_T = 1$ MΩ and $C_G + C_T = 4$ aF).

As the current contour plot (see Fig. 2) can also be treated as input–output characteristics of a CBS, it can be said that energy quantization increases the voltage level by an amount $\Delta V_{DS} = \Delta E/q$ and the periodicity by an amount $\Delta V_{GS} = C_\Sigma \Delta E/qC_G$ of a CBS output. At the same time, as the slope $(\partial V_{DS}/\partial V_{GS})$ of the equations $\Delta F = 0$ does not depend on ΔE, it is inferred that the gain of CBS is independent of energy quantization. It is noteworthy that the increase of Coulomb blockade area due to energy quantization has been experimentally demonstrated by Saitoh and Hiramoto [12].

The MC simulation results reported in this paper often took several days (as a specific example, the drain current contour simulation (see Fig. 2) took 4 days 18 h 28 min to complete on a 64-bit octacore Linux server, with all the jobs multithreaded and submitted parallely in all the cores dedicated just for this paper). Hence, the compact analytical models developed in this paper will be of immense use to potential circuit designers, as discussed in the following sections.

B. *Energy Quantization Effects on the SET Inverter*

In this paper, we analyzed the effect of energy quantization on the voltage-state SET logic inverter, which was described in [13]. Fig. 3 shows the influence of energy quantization on SET inverter transfer ($V_{\rm OUT}$ versus $V_{\rm IN}$) characteristics and also indicates that increasing energy quantization ΔE shifts the inverter characteristics toward the right, thus implying that larger input voltage $V_{\rm IN}$ is required for switching of a nonmetallic SET with quantized energy states than its metallic counterpart. This is analogous to the influence of fixed positive background charges in the island, as described in [13]. It might be possible to compensate this horizontal shift by adding a second gate to the SET island with appropriate control bias. Fig. 4 demonstrates the fact that increasing supply voltage degrades the inverter performance. Therefore, the supply voltage values $V_{DD} = -V_{SS} = q/2\,(C_G + C_T)$, which are optimum [1] for the metallic SET inverter, also appear to be optimum in presence of energy quantization. Fig. 5 shows the influence of energy quantization on power-delay product of the SET inverter. Here, power dissipation is static in nature and is calculated as $(V_{DD} - V_{SS})\,I_{\rm STATIC}$, where $I_{\rm STATIC}$ is the steady-state cur-

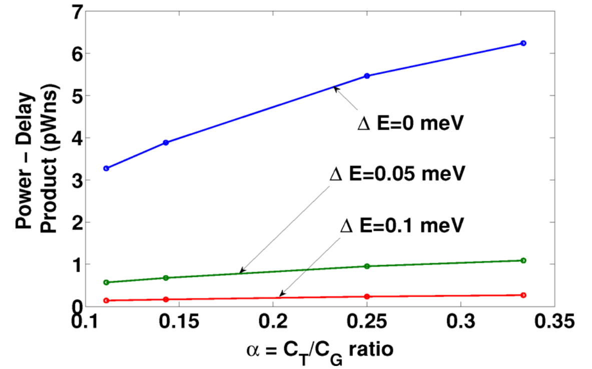

Fig. 5. Variation of power-delay product (in pWns) with capacitance ratio $\alpha = C_T/C_G$ using different values of energy quantization ΔE (in millielectronvolts) as a metric.

rent flowing from V_{DD} to V_{SS} [1], [13]. The inverter delay increases and power dissipation decreases as the drive current decreases with increasing ΔE.

C. *Modeling of Inverter Noise Margin*

The expressions for orthodox noise margin (NM) parameters were derived in [13] as

$$V_{OH} = -V_{OL} = \frac{\alpha V_{DD}}{2\alpha^2 + \alpha + 1} \tag{10}$$

$$V_{IH} = -V_{IL} = \frac{\alpha^2 V_{DD}}{2\alpha^2 + \alpha + 1} \tag{11}$$

$$NM = NM_H = NM_L = \frac{\alpha\,(1-\alpha)\,V_{DD}}{2\alpha^2 + \alpha + 1}. \tag{12}$$

Inclusion of energy quantization alters the previous noise margin parameters into the following expressions (see the Appendix):

$$\left\{ \begin{matrix} V'_{OH} \\ V'_{OL} \end{matrix} \right\} = \left\{ \begin{matrix} V_{OH} \\ V_{OL} \end{matrix} \right\} - \left(\frac{1}{2\alpha^2 + \alpha + 1} \right) \frac{\Delta E}{q} \tag{13}$$

$$\left\{ \begin{matrix} V'_{IH} \\ V'_{IL} \end{matrix} \right\} = \left\{ \begin{matrix} V_{IH} \\ V_{IL} \end{matrix} \right\} + \left(\frac{2\alpha^2 + 2\alpha + 1}{2\alpha^2 + \alpha + 1} \right) \frac{\Delta E}{q}. \tag{14}$$

Throughout this paper, *primed variables* $(')$ refer to the quantities including energy quantization effects, while

Authorized licensed use limited to: INDIAN INSTITUTE OF SCIENCE. Downloaded on January 13, 2010 at 00:50 from IEEE Xplore. Restrictions apply.

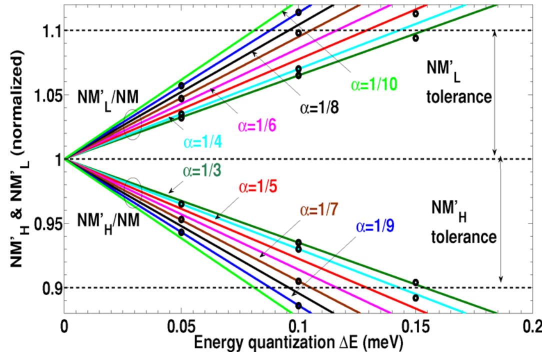

Fig. 6. Variation of normalized noise margins NM'_H/NM and NM'_L/NM of the SET inverter with energy quantization ΔE for different $\alpha = C_T/C_G$ ratios at constant $V_{DD} = 20$ mV bias. The symbols represent simulated data while solid lines indicate the results predicted by the model (noise margin tolerance is taken as 10% of the orthodox value).

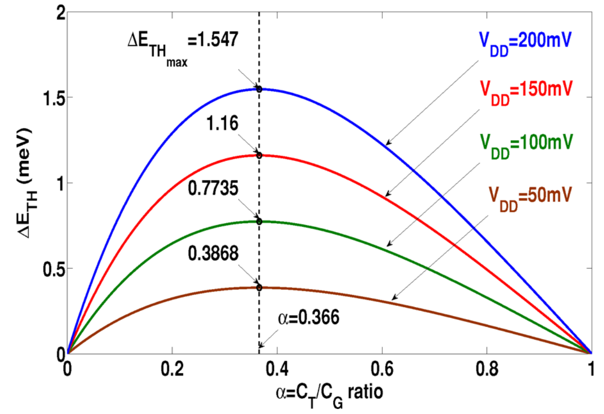

Fig. 7. Variation of quantization threshold $\Delta E_{\rm TH}$ as a function of $\alpha = C_T/C_G$ ratio for a noise tolerance of 10% of the orthodox noise margin (i.e., $x = 0.1$). Note that $(C_G + C_T)$ value is decreased (considering SET devices with smaller dimensions) proportionally with increase in V_{DD}.

unprimed variables refer to the ideal classical situation with the metallic SETs, following the orthodox theory of single-electron tunneling. Equation (14) indicates that the entire transfer characteristics shift toward the right by the amount $\Delta E\left(2\alpha^2+2\alpha+1\right)/\left(2\alpha^2+\alpha+1\right)q$ with respect to the orthodox characteristics. Equation (13) shows that both the output voltage levels decrease simultaneously by $\Delta E/\left(2\alpha^2+\alpha+1\right)q$.

From the basic definitions of noise margins $NM_H \triangleq V_{OH} - V_{IH}$ and $NM_L \triangleq V_{IL} - V_{OL}$, we obtain

$$\begin{Bmatrix} NM'_H \\ NM'_L \end{Bmatrix} = NM \mp 2\left(\frac{\alpha^2+\alpha+1}{2\alpha^2+\alpha+1}\right)\frac{\Delta E}{q}. \quad (15)$$

From (15), it is evident that energy quantization increases the noise margin for low logic and decreases the noise margin for high logic by the same amount $2\Delta E\left(\alpha^2+\alpha+1\right)/\left(2\alpha^2+\alpha+1\right)q$. Thus, it is seen that for the continuous spectrum ($\Delta E = 0$), (15) reduces to the orthodox model of noise margin, as proposed in [13].

From the inverter transfer characteristics simulated in SIMON for different α and ΔE, the values of V_{OH}, V_{OL}, V_{IH}, and V_{IL} are recorded and the corresponding NM_H and NM_L are calculated. In Fig. 6, these values are plotted and the variation of normalized noise margins with energy quantization is shown. Fig. 6 also demonstrates the excellent agreement between the proposed model (15) and the simulated results. Here, we introduce a parameter *quantization threshold* ($\Delta E_{\rm TH}$), which may be defined as the maximum allowable energy quantization, for a given capacitance ratio $\alpha = C_T/C_G$, which the SET logic circuit can withstand before the noise margin falls below a specific tolerable value. Equating the relation for noise margin with any specified value of noise tolerance (x%) and putting the expression of orthodox noise margin NM from (12) in (15), we finally obtain

$$\Delta E_{\rm TH} = \frac{qx\alpha\left(1-\alpha\right)V_{DD}}{2\left(\alpha^2+\alpha+1\right)}. \quad (16)$$

The optimal $\alpha = C_T/C_G$ ratio of the SET inverter circuit for which the maximum robustness can be achieved is calculated by maximizing (16). Now, by solving $\partial\Delta E_{\rm TH}/\partial\alpha = 0$, it is found that the condition for achieving maximum robustness against energy quantization effects occurs at $\alpha = \left(\sqrt{3}-1\right)/2 = 0.366$ and the maximum quantization threshold $\Delta E_{\rm TH_{max}}$ an SET logic circuit can tolerate is given as

$$\Delta E_{\rm TH_{max}} = \Delta E_{\rm TH}\Big|_{@\alpha=0.366} = \frac{qxV_{DD}}{13}. \quad (17)$$

Equation (16) is plotted in Fig. 7, where it is shown that the SET inverter can withstand the maximum $\Delta E_{\rm TH_{max}}$ of $qxV_{DD}/13$ at the optimum C_T/C_G ratio of 0.366. It is worth noting that in our earlier work [13], we have shown that $C_T/C_G = 1/3$ design criteria also provide maximum robustness against background charge and device parameter variation. On the other hand, for a given bias V_{DD} and ΔE, the value of α, for which one can get maximum noise margins, is obtained from the relations $\partial NM'_{H_{\max}}/\partial\alpha = 0$ and $\partial NM'_{L_{\max}}/\partial\alpha = 0$ as

$$\alpha(\Delta E)\Bigg|_{\begin{Bmatrix} NM'_{H_{\max}} \\ NM'_{L_{\max}} \end{Bmatrix}} = \left[\pm 1 + \sqrt{\left(\frac{qV_{DD}}{\Delta E}\right)^2 + 1 \mp \frac{3}{2}\left(\frac{qV_{DD}}{\Delta E}\right)} - \frac{1}{2}\left(\frac{qV_{DD}}{\Delta E}\right)\right] \Bigg/ \left[\frac{3}{2}\left(\frac{qV_{DD}}{\Delta E}\right) \mp 1\right]. \quad (18)$$

Here, $(+,-,-)$ sequence is used for $NM'_{H_{\max}}$ and $(-,+,+)$ sequence is used for $NM'_{L_{\max}}$. Equation (18) is plotted in Fig. 8, which shows that for high $V_{DD}/\Delta E$ values, the noise margins NM'_H and NM'_L asymptotically merge together at the orthodox noise margin NM, and this occurs at $\alpha \approx 1/3$. From this figure, it can also be concluded that in the presence of energy quantization, it is not possible to optimize both noise margins simultaneously by tuning the α parameter. The maximum operable temperature for using voltage-state SET-based inverter logic

Authorized licensed use limited to: INDIAN INSTITUTE OF SCIENCE. Downloaded on January 13, 2010 at 00:50 from IEEE Xplore. Restrictions apply.

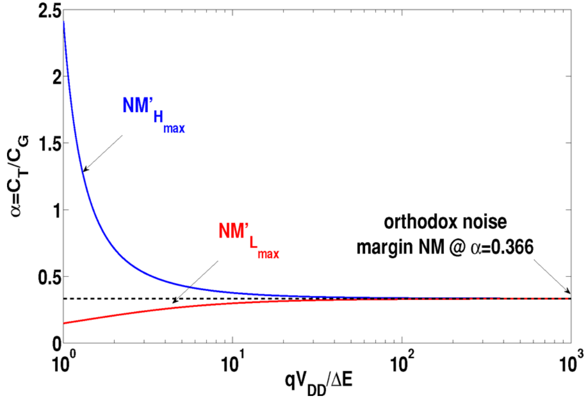

Fig. 8. Variation of $\alpha = C_T/C_G$ ratio as a function of the ratio $qV_{DD}/\Delta E$, indicating the value of α necessary at a given bias V_{DD} and energy quantization ΔE to obtain maximum noise margins.

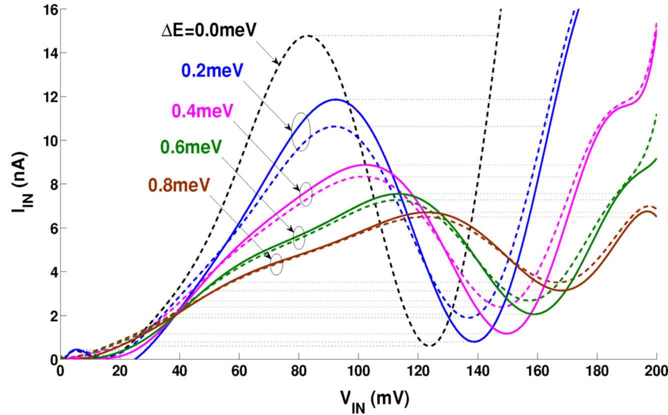

Fig. 9. Influence of energy quantization and temperature on $I_{\rm IN} - V_{\rm IN}$ characteristics of the NDR circuit. The solid and the broken lines represent the plots at temperatures 40 and 80 K, respectively. The minor dotted lines represent the path followed by the circuit during operation, giving rise to the hysteresis shown in Fig. 10 (simulated for $I_{\rm BIAS} = 5$ nA, $R_T = 1$ MΩ, $C_G = 0.5$ aF, and $C_T = 0.25$ aF).

circuits was demonstrated earlier [1], [13] as $T_{\max} < q^2/40k_BC_\Sigma$, which implies $T \approx 11.6$ K for $C_\Sigma = 4$ aF. As the noise margin does not change with temperature in this operating regime, we have not included the temperature term in the proposed model. The amount of energy quantization could be reduced by increasing the doping concentration of the island.

D. Effects of Energy Quantization on the NDR Circuit

CBS is an integral part of almost all CMOS-SET hybrid circuits. First, we discuss the effects of energy quantization on NDR (and corresponding hysteresis circuit), which was proposed by Mahapatra and Ionescu [4], [5]. Fig. 9 shows the influence of energy quantization on the $I_{\rm IN} - V_{\rm IN}$ characteristics of the CBS-based NDR circuit. It indicates that increasing energy quantization ΔE as well as increasing temperature decreases the dynamic range as well as the slope (conductance) of the NDR region. Also, the peak position of the NDR is shifting toward the higher $V_{\rm IN}$ values as the x-coordinate of A_n increases with energy quantization.

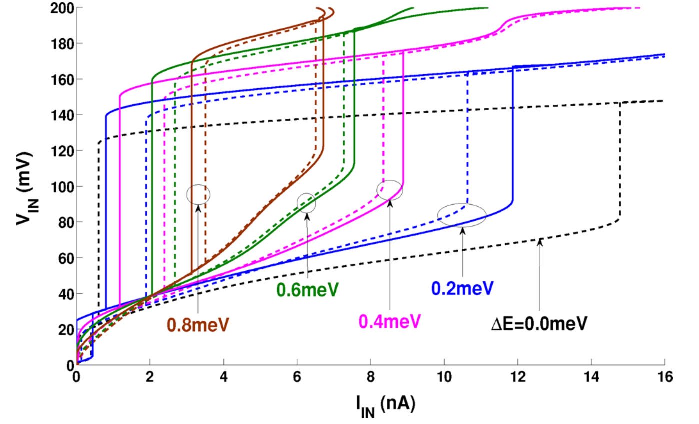

Fig. 10. Effect of energy quantization on the current hysteresis characteristics. The solid and the broken lines represent the plots at temperatures 40 and 80 K, respectively (simulated for $I_{\rm BIAS} = 5$ nA, $R_T = 1$ MΩ, $C_G = 0.5$ aF, and $C_T = 0.25$ aF).

Considering only the most probable electron tunneling events ($0 \leftrightarrow 1$ transitions) in the SETs using the Mahapatra, Ionescu, and Banerjee (MIB) model [2], the net current through the NDR may be written as

$$I_{\rm IN} = \frac{1}{R_T V_{\rm IN}} \left[\frac{C_G + C_T}{C_\Sigma} V_{\rm IN} - \frac{C_G}{C_\Sigma} V_{\rm OUT} + \alpha\right] \times \left[\frac{C_T}{C_\Sigma} V_{\rm IN} + \frac{C_G}{C_\Sigma} V_{\rm OUT} - \alpha\right] \quad (19)$$

where $\alpha = (q/2C_\Sigma + \Delta E/q)$ and $V_{\rm OUT}$ is the output of CBS. Equation (19) is differentiated with respect to $V_{\rm IN}$ to obtain

$$R_T C_\Sigma^2 \frac{\partial I_{\rm IN}}{\partial V_{\rm IN}} = \frac{\partial V_{\rm OUT}}{\partial V_{\rm IN}} \left[C_G^2 + \frac{2\alpha C_G C_\Sigma}{V_{\rm IN}} - \frac{2C_G^2 V_{\rm OUT}}{V_{\rm IN}}\right] + \frac{\alpha^2 C_\Sigma^2}{V_{\rm IN}^2} + \frac{C_G^2 V_{\rm OUT}^2}{V_{\rm IN}^2} - \frac{2\alpha C_G C_\Sigma V_{\rm OUT}}{V_{\rm IN}^2} + C_T (C_G + C_T). \quad (20)$$

Replacing $V_{GS} = V_{\rm OUT}$ and $V_{DS} = V_{\rm IN}$ in (6) and differentiating it, we get $\partial V_{\rm OUT}/\partial V_{\rm IN} = (C_G + C_T)/C_G$, and using (5) and (6), we finally obtain the following form:

$$\frac{\partial I_{\rm IN}}{\partial V_{\rm IN}} = \frac{\alpha^2}{R_T V_{\rm IN}^2} = \frac{1}{R_T V_{\rm IN}^2} \left(\frac{q}{2C_\Sigma} + \frac{\Delta E}{q}\right)^2. \quad (21)$$

It should be noted that (12) is derived from the MIB model, which based on the orthodox theory, and hence, it is valid for $\Delta E \ll q^2/C_\Sigma$ (small perturbation). Similar to the NM model, (12) does not contain any temperature term, since they hold good for $T < q^2/40k_BC_\Sigma$. The NDR circuit can also be used as a hysteresis loop circuit [5], and the effect of energy quantization on the loop area is shown in Fig. 10. As the NDR region degrades with ΔE, the area of the hysteresis loop also reduces. The effects of energy quantization on CBS circuits could be compensated by reducing the bias current. It is worth noting that in CBS-based circuits, we use smaller values of C_Σ in comparison to

Authorized licensed use limited to: INDIAN INSTITUTE OF SCIENCE. Downloaded on January 13, 2010 at 00:50 from IEEE Xplore. Restrictions apply.

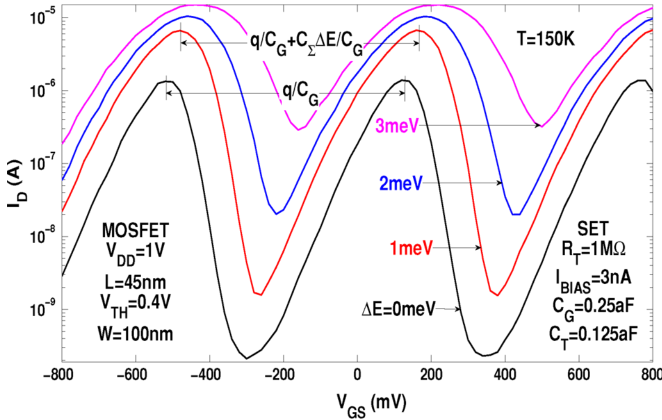

Fig. 11. Effect of the energy quantization on the SETMOS characteristics. Here, V_{GS} and I_{DS} refer to gate voltage of SET and drain current of MOSFET, respectively, as explained in [6].

the SET inverter, and thus, the values of ΔE in CBS circuits are taken to be higher than the inverter circuits.

E. Effect of Energy Quantization on the SETMOS Circuit

SETMOS [6] is a hybrid CMOS-SET architecture that offers Coulomb blockade oscillation at much higher current level than normal SET. As the MOSFET is operated in the subthreshold region, the output drain current exponentially amplifies the oscillations of the drain voltage of the CBS, and the amount of current amplification depends on the MOSFET feature size. Fig. 11 shows the effects of energy quantization on the SETMOS circuit. The output of CBS is first simulated with SIMON, and then fed to AIMSPICE [14] in order to obtain the SETMOS characteristics. In AIMSPICE, we use a 45-nm high-performance (HP) BSIM predictive technology model [15] card to simulate the MOSFET behavior. In this simulation, we neglected the MOSFET's gate leakage current since in this model card, the gate current (approximately in picoamperes) is found to be much smaller than SET bias current (approximately in nanoamperes). It is observed that with the increase of ΔE, both the peak and valley currents increase; however, the peak-to-valley ratio decreases.

IV. Conclusion

In this paper, the effects of energy quantization on SET devices and circuits are studied using analytical models and MC simulation. Including the energy quantization term, a new noise margin model for the SET inverter is proposed, and then used to study the robustness of the SET inverter against energy quantization effects. It is found that the SET inverter designed with $C_T : C_G \sim 0.366$ offers the maximum robustness against energy quantization, and the maximum tolerable value of energy quantization is found to be $(qxV_{DD}/13)$ eV for $x\%$ tolerance over the orthodox noise margin. Impact of energy quantization is then studied for two CBS circuits: pure SET-based NDR and hybrid CMOS-SET-based SETMOS circuit. It is observed that, in general, the energy quantization degrades the performances of SET circuits.

Appendix

Energy quantization shifts the transfer characteristics toward the right. One can simplify the calculations by shifting the origin of the inverter transfer characteristics (which was at $V_{\rm IN} = 0$ in the orthodox model) to $V'_{\rm IN} = V_{\rm IN} - \Delta E/q$. The transfer characteristics of a typical voltage-state SET inverter is $V^3_{\rm OUT} + A_2 V^2_{\rm OUT} + A_1 V_{\rm OUT} + A_0 = 0$ [1], [13]. For a voltage-state SET inverter, $V^3_{\rm OUT} + A_2 V^2_{\rm OUT}$ term is much smaller than $A_1 V_{\rm OUT} + A_0$, and hence, one can linearize it as $A_1 V_{\rm OUT} + A_0 = 0$. Now, including the energy quantization term ΔE, the coefficients A_0 and A_1 change from the standard orthodox forms into

$$A'_1 = A_1 - \frac{q^2}{4C_T (C_G + C_T)^3} \left[\frac{2C_G \Delta E \left(C_G^2 - C_T^2\right)}{q^2} + \frac{4C_G^2 \Delta E^2 (C_G + C_T)^2}{q^4} \right] \tag{22}$$

$$A'_0 = A_0 \left[1 - \frac{2C_G (C_G + C_T) \Delta E}{q^2 C_T} \right]. \tag{23}$$

Using (22) and (23) in $A'_1 V'_{\rm OUT} + A'_0 = 0$, one obtains the expressions for V'_{OH} and V'_{OL} as

$$\begin{matrix} V'_{OH} \\ V'_{OL} \end{matrix} = \pm C_G V_{DD} \left[\frac{C_T - 2C_G (C_G + C_T) \Delta E / q^2}{C_G^2 + C_G C_T + 2C_T^2} \right]. \tag{24}$$

The slope of the transfer characteristics in the transition region is given as

$$\frac{\partial V_{\rm OUT}}{\partial V_{\rm IN}} = -\frac{C_G}{C_T} = \frac{V'_{OH}}{V'_{IL} - \Delta E / q}. \tag{25}$$

Using this slope formulation, one can obtain the expressions for V'_{IL} and V'_{IH} as

$$\begin{matrix} V'_{IL} \\ V'_{IH} \end{matrix} = \Delta E \mp C_T V_{DD} \left[\frac{C_T - 2C_G (C_G + C_T) \Delta E / q^2}{C_G^2 + C_G C_T + 2C_T^2} \right]. \tag{26}$$

References

[1] S. Mahapatra and A. M. Ionescu, *Hybrid CMOS Single Electron Transistor Device and Circuit Design*. Norwood, MA: Artech House, 2006.
[2] S. Mahapatra, V. Vaish, C. Wasshuber, K. Banerjee, and A. M. Ionescu, "Analytical modeling of single electron transistor for hybrid CMOS-SET analog IC design," *IEEE Trans. Electron. Devices*, vol. 51, no. 11, pp. 1772–1782, Nov. 2004.
[3] K. K. Likharev, "Single-electron devices and their applications," *Proc. IEEE*, vol. 87, no. 4, pp. 606–632, Apr. 1999.
[4] S. Mahapatra and A. M. Ionescu, "A novel elementary SET negative differential resistance device," *Jpn. J. Appl. Phys.*, vol. 43, no. 2, pp. 538–539, 2004.
[5] S. Mahapatra, V. Pott, and A. M. Ionescu, "Few electron negative differential resistance (NDR) devices," in *Proc. Int. Semicond. Conf. (CAS)*, 2003, vol. 1, pp. 51–54.
[6] A. M. Ionescu, S. Mahapatra, and V. Pott, "Hybrid SETMOS architecture with Coulomb blockade oscillations and high current drive," *IEEE Electron. Device Lett.*, vol. 25, no. 6, pp. 411–413, Jun. 2004.
[7] C. Wasshuber, H. Kosina, and S. Selberherr, "SIMON—A simulator for single-electron tunnel devices and circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 16, no. 9, pp. 937–944, Sep. 1997.
[8] H. Grabert and M. H. Devoret, Eds., *Single Charge Tunneling, Coulomb Blockade Phenomena in Nanostructures* (NATO ASI Series). New York: Plenum, 1992.

Authorized licensed use limited to: INDIAN INSTITUTE OF SCIENCE. Downloaded on January 13, 2010 at 00:50 from IEEE Xplore. Restrictions apply.

[9] C. Wasshuber, *Computational Single-Electronics*. New York: Springer-Verlag, 2001, 2010.
[10] S. Datta, "Electronic transport in mesoscopic systems," in *Cambridge Studies in Semiconductor Physics and Microelectronic Engineering*. Cambridge, U.K.: Cambridge Univ. Press, 1997.
[11] K. Miyaji, M. Saitoh, and T. Hiramoto, "Compact analytical model for room-temperature operating silicon single-electron transistors with discrete quantum levels," *IEEE Trans. Nanotechnol.*, vol. 5, no. 3, pp. 167–173, May 2006.
[12] M. Saitoh and T. Hiramoto, "Extension of Coulomb blockade region by quantum confinement in the ultrasmall silicon dot in a single-hole transistor at room temperature," *Appl. Phys. Lett.*, vol. 84, no. 16, pp. 3172–3174, 2004.
[13] C. Sathe, S. S. Dan, and S. Mahapatra, "Assessment of SET logic robustness through noise margin modeling," *IEEE Trans. Electron. Devices*, vol. 55, no. 3, pp. 909–915, Mar. 2008.
[14] *AIM-Spice Users' Manual* [Online]. Available: http://www.aimspice.com/
[15] *BSIM Predictive Technology Model* [Online]. Available: http://www.eas.asu.edu/ptm/

Surya Shankar Dan was born in Kolkata, India, on March 14, 1983. He received the B.Eng. degree in electronics and telecommunications engineering and the M.Eng. degree specializing in microelectronic devices from the Department of Electronics and Telecommunications Engineering, Jadavpur University, Kolkata, in 2004 and 2006, respectively. He is currently working toward the Ph.D. degree at the Centre for Electronics, Design and Technology, Indian Institute of Science, Bengaluru, India.

He is engaged in research on the impact of energy quantization on single-electron devices and circuits. His current research interests include quantum transport in the mesoscopic regime and the development of physics-based compact analytical models for advanced CMOS and beyond CMOS nanoscale electronic device technologies.

Santanu Mahapatra (M'08) received the B.E. degree in electronics and telecommunication from Jadavpur University, Kolkata, India, in 1999, the M.Tech. degree in electrical engineering with specialization in microelectronics from the Indian Institute of Technology (IIT), Kanpur, India, in 2001, and the Ph.D. degree in electrical engineering from the Swiss Federal Institute of Technology Lausanne (EPFL), Lausanne, Switzerland, in 2005. He was engaged in research on compact modeling of single-electron transistors and their hybridization with CMOS.

In 2006, he founded the Nano-Scale Device Research Laboratory, Centre for Electronics Design and Technology (CEDT), Indian Institute of Science, Bengaluru, India, where he has been an Assistant Professor since 2005, and is engaged in research on compact modeling and simulation of emerging nanotechnologies and advanced CMOS devices. He provides consultancy to the device reliability group of Cypress Semiconductor, Bengaluru. He is the author or coauthor of several papers published in international journals and refereed conferences. He is also the author of the book *Hybrid CMOS Single Electron Transistor Device and Circuit Design* (Artech House, 2006). His current research interests include device reliability, multigate transistors, tunnel field-effect transistors, single-electron transistors, and CMOS-nanohybridization.

Dr. Mahapatra received the Best Paper Award in the International Semiconductor Conference (CAS), Romania, in 2003. He is also the recipient of the International Business Machines Corporation (IBM) Faculty Award in 2007 and the Microsoft India Research Outstanding Faculty Award in 2007.

Authorized licensed use limited to: INDIAN INSTITUTE OF SCIENCE. Downloaded on January 13, 2010 at 00:50 from IEEE Xplore. Restrictions apply.