

Piecewise Linearization Technique for Compact Charge Modeling of Independent DG MOSFET

Srivatsava Jandhyala, Aby Abraham, Costin Anghel, *Member, IEEE*, and Santanu Mahapatra, *Senior Member, IEEE*

Abstract—Charge linearization techniques have been used over the years in advanced compact models for bulk and double-gate MOSFETs in order to approximate the position along the channel as a quadratic function of the surface potential (or inversion charge densities) so that the terminal charges can be expressed as a compact closed-form function of source and drain end surface potentials (or inversion charge densities). In this paper, in case of the independent double-gate MOSFETs, we show that the same technique could be used to model the terminal charges quite accurately only when the 1-D Poisson solution along the channel is fully hyperbolic in nature or the effective gate voltages are same. However, for other bias conditions, it leads to significant error in terminal charge computation. We further demonstrate that the amount of nonlinearity that prevails between the surface potentials along the channel actually dictates if the conventional charge linearization technique could be applied for a particular bias condition or not. Taking into account this nonlinearity, we propose a compact charge model, which is based on a novel piecewise linearization technique and shows excellent agreement with numerical and Technology Computer-Aided Design (TCAD) simulations for all bias conditions and also preserves the source/drain symmetry which is essential for Radio Frequency (RF) circuit design. The model is implemented in a professional circuit simulator through Verilog-A, and simulation examples for different circuits verify good model convergence.

Index Terms—Circuit simulation, compact modeling, double-gate MOSFET, terminal charge.

I. INTRODUCTION

THE independent double-gate (IDG) MOSFET has attracted much attention due to its ability to modulate the threshold voltage and transconductance dynamically that leads to novel circuit applications, as demonstrated in the literatures [1]–[4]. An accurate compact model of the terminal charges applicable for all bias conditions for such devices are needed to conduct transient and small-signal analysis in a circuit simulator. As the terminal charge integrals cannot be directly solved, different charge linearization techniques are developed over the years (first for bulk [5], [6] and then for DG [7]–[9] MOSFETs)

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to approximate the position along the channel as a quadratic function of the surface potential (or inversion charge densities) so that the terminal charges can be expressed as a compact closed-form function of source and drain end surface potentials (or inversion charge densities). In this paper, we show that for IDG MOSFETs, the same technique cannot be used for all bias conditions. Analyzing the nonlinearity between two surface potentials, we demonstrate that the existing model [9] predicts the transcapacitance values accurately when the nonlinearity between two surface potentials is small (which happens when the potential solution throughout the channel is hyperbolic in nature or the effective gate voltages are equal); however, there is a significant inaccuracy in prediction when the nonlinearity is large (which happens when the potential solution throughout the channel is fully or partially trigonometric in nature). We then propose a compact charge model that takes into account this nonlinearity through a novel piecewise linearization technique. The proposed model, which shows excellent agreement with numerical and TCAD simulations in all bias conditions, is successfully implemented in a professional circuit simulator through Verilog-A interface and also preserves the source/drain symmetry which is essential for RF circuit design.

II. MODEL DEVELOPMENT

A. Limitations of Existing Models

Let us consider an IDG MOSFET having gate oxide thicknesses of $t_{ox1(2)}$, a silicon body thickness of t_{si} , a channel length of L , and a channel width of W . The “exact” drain current equation for the device could be written as [10]

$$I_{ds} = \mu \frac{W}{L} [F(Q_{i1s}, Q_{i2s}, G_s) - F(Q_{i1d}, Q_{i2d}, G_d)] \quad (1)$$

where

$$F(Q_{i1}, Q_{i2}, G) = \frac{Q_{i1}^2}{2C_{ox1}} + \frac{Q_{i2}^2}{2C_{ox2}} + \frac{2}{\beta}(Q_{i1} + Q_{i2}) + \frac{1}{2}\epsilon_{si}t_{si}G. \quad (2)$$

Here, Q_{i1} and Q_{i2} are the inversion charge densities of the first and second gates given by

$$Q_{i1(2)} = C_{ox1(2)} (V_{g1(2)} - \psi_{1(2)}) \quad (3)$$

and G , the coupling factor is expressed as [11]

$$G = \frac{Q_{i1}^2}{\epsilon_{si}^2} - Be^{\beta(\psi_1 - V)} = \frac{Q_{i2}^2}{\epsilon_{si}^2} - Be^{\beta(\psi_2 - V)}. \quad (4)$$

Here, $C_{ox1(2)}$ are the oxide capacitance per unit area of first(second) gate defined as $\epsilon_{ox}/t_{ox1(2)}$, C_{si} is the silicon body

capacitance per unit area defined as $\epsilon_{\text{si}}/t_{\text{si}}$, ϵ_{si} and ϵ_{ox} are the permittivities of Si and SiO_2 respectively, q is the elementary charge, β is the inverse thermal voltage, n_i is the intrinsic carrier density, $B = 2qn_i/\beta\epsilon_{\text{si}}$, $\psi_{1(2)}$ are the Si/SiO₂ surface potentials at first(second) gate, V is the electron quasi-Fermi potential (channel potential), $V_{g1(2)}$ is the effective gate voltage (i.e., $V_{g1(2)} = V_{g\text{applied}} - \delta\phi_{1(2)}$, where $V_{g\text{applied}}$ is the voltage applied at the gate terminal, and $\delta\phi_{1(2)}$ is the work-function difference between the gate material and silicon), and μ is the effective mobility. In all the discussion that follows, any variable with subscript “ s ” refers to its values at source end, and any variable with subscript “ d ” refers to its value at drain end. We also use the following terminologies to define the “state” of the channel:

HH: nature of the P-IVE¹ is hyperbolic at both source and drain ends.

TT: nature of the P-IVE is trigonometric at both source and drain ends.

TH: nature of the P-IVE is trigonometric at the source end but hyperbolic at the drain end.

Now, the position y along the channel ($y = 0$ describes the source end, and $y = L$ denotes the drain end) can be related to the inversion charge densities (Q_{i1} and Q_{i2}) at that point by the following relationship [12]:

$$\frac{y}{L} = \frac{F_s - F}{F_s - F_d} \quad (5)$$

where $F_s = F(Q_{i1s}, Q_{i2s}, G_s)$ and $F_d = F(Q_{i1d}, Q_{i2d}, G_d)$. According to the Ward–Dutton charge partition theory [13], terminal charges could be given as

$$Q_{G1} = W \int_0^L Q_{i1}(y) dy \quad (6)$$

$$Q_{G2} = W \int_0^L Q_{i2}(y) dy \quad (7)$$

$$Q_D = -W \int_0^L \frac{y}{L} Q_i(y) dy \quad (8)$$

$$Q_S = -(Q_{G1} + Q_{G2} + Q_D) \quad (9)$$

where Q_i represents the total inversion charge density ($= Q_{i1} + Q_{i2}$). As the exact integration of (6)–(9) are not available, several charge linearization techniques [5]–[9] have been proposed so that y (or F) in (5) could be approximated as a quadratic function of $\psi_{1(2)}$ (or $Q_{i1(2)}$), which results in a closed-form expression of terminal charges.

However, from (2), one can see that, irrespective of the linearization technique, in order to approximate F as a quadratic function of either ψ_1 or ψ_2 , for a given bias condition, ψ_1 has to

linearly change with ψ_2 along the channel. Those two surface potentials hold a linear relationship only for the following two bias conditions.

- 1) When the channel is HH in nature: In this case, potential distribution is monotonous in the direction perpendicular to the channel, and one surface is always in weak inversion.
- 2) When the effective gate voltages are equal (i.e., common gate device having the same gate work function but could have difference in oxide thickness) [14]. It is a special case under TT state.

In other cases (i.e., TH or TT), there would be certain amount of nonlinearity factor (NLF) between ψ_1 and ψ_2 , and depending on the value of NLF , a quadratic approximation of F as a function of ψ_1 or ψ_2 might lead to significant error in terminal charge calculation.

From Fig. 1(a), one can see that there is disagreement between y versus ψ_1 relationship predicted by the model [9] and the numerical simulation when the relationship between ψ_1 and ψ_2 is nonlinear. This results in significant disagreement in transcapacitance values when the NLF is high, as demonstrated in Fig. 1(b) and (c). At the same time, the model shows good agreement with numerical data for small values of NLF . It is also shown that NLF is much higher in TH and TT mode in comparison to the HH mode. Here, NLF is calculated as [14], [15]

$$NLF = \frac{\sqrt{\int_{\psi_{1s}}^{\psi_{1d}} [\psi_2 - \tilde{\psi}_2]^2 d\psi_1}}{\psi_{1d} - \psi_{1s}} \quad (10)$$

where $\tilde{\psi}_2$ is the linear approximation of the exact ψ_2 . It should be also noted that the $(1/2)\epsilon_{\text{si}}t_{\text{si}}G$ term in (1) does not contribute much in total drain current. Therefore, the exact nature of relationship between G and $\psi_{1(2)}$ does not have any significant impact on terminal charge calculation. In passing, we also like to mention that the effect of NLF on the model is not equally visible to all transcapacitance values. It has a very strong impact on C_{g1g2} (or C_{g2g1}) and C_{gkd} (where $k = 1$ if $V_{g1} < V_{g2}$ else $k = 2$) characteristics and lesser impact on other transcapacitance values. It is also found that the value of NLF and its impact on the existing model [9] increases with the bias.

B. Proposed Charge Model

In order to apply the conventional charge linearization technique for all bias conditions, we propose “piecewise linearization” technique, where we divide channel into segments in such a way that ψ_1 and ψ_2 hold a quasi-linear relationship in each segment. The expressions for the partial terminal charges, i.e., terminal charges computed only for the p th segment, can be obtained by modifying the expressions in [14] as

$$Q_{G_k}^p = [Q_{G_k}^{p_{\text{lo}}} + Q_{G_k}^{p_{\text{hi}}}] \quad (k = 1 \text{ or } 2) \quad (11)$$

$$Q_D^p = \left[\frac{L^p}{L} (Q_D^{p_{\text{lo}}} + Q_D^{p_{\text{hi}}}) - \frac{y^p}{L} \left(\sum_{k=1}^2 Q_{G_k}^p \right) \right] \quad (12)$$

¹In this paper, the surface potential equations proposed in [11] are called primary input voltage equations (P-IVE). Another set of implicit equations will be introduced in the next section, which will be called secondary input voltage equations (S-IVE).

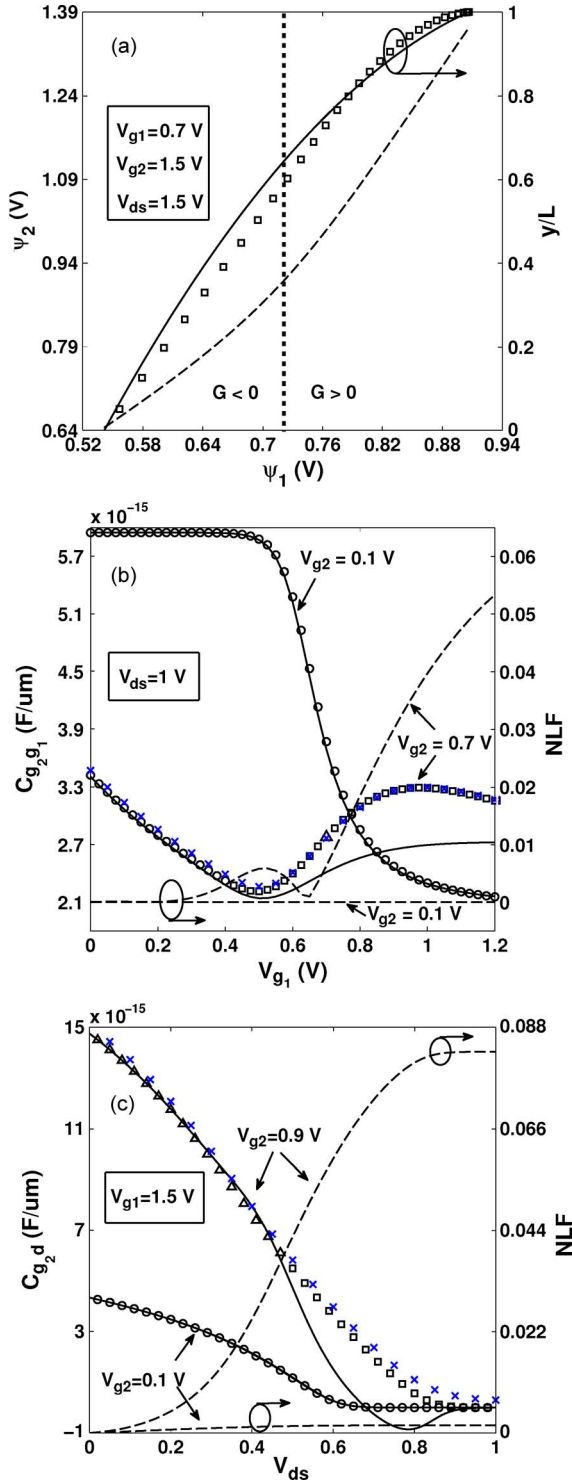


Fig. 1. (a) Left axis depicts the variation of ψ_2 with ψ_1 along the channel. At each ψ_1 , right axis shows the y/L predicted by [9] (solid line) and the exact value obtained from numerical simulation (symbol). (b) Left axis compares the transcapacitance $C_{g_2g_1}$ characteristics predicted by [9] (solid lines) with the exact values obtained from numerical simulation (symbol) for two different V_{g2} biases. Right axis depicts their respective NLF (dotted lines). (c) Left axis compares the transcapacitance C_{g_2d} characteristics predicted by [9] (solid lines) with the exact values obtained from numerical simulation (symbol) for two different biases. Right axis depicts the NLF (dotted lines) for each of these cases. In the figure, the “state” of the channel at any bias point is depicted by varying the symbol used for numerical simulation: circle represents HH, square represents TH, and triangle represents TT. TCAD simulation data (crosses) are shown for few cases to preserve the clarity. Device used has $t_{ox1} = 1.5$ nm, $t_{ox2} = 1$ nm, and $t_{si} = 10$ nm.

where

$$Q_{G_k}^{plo} = WLP \left[\frac{Q_{iky^p} + Q_{iky^{p+1}}}{2} \right] \quad (13)$$

$$Q_D^{plo} = -WLP \sum_{k=1}^2 \left[\frac{Q_{iky^p}}{6} + \frac{Q_{iky^{p+1}}}{3} \right] \quad (14)$$

$$Q_{G_k}^{phi} = WLP \left[\frac{\nu_k^p (Q_{iky^p} - Q_{iky^{p+1}})^2}{6(\nu_k^p (Q_{iky^p} + Q_{iky^{p+1}}) + \lambda_k^p)} \right] \quad (15)$$

$$Q_D^{phi} = -WLP \sum_{k=1}^2 \left[\nu_k^p (Q_{iky^p} - Q_{iky^{p+1}})^2 \times \frac{(5\lambda_k^p + 6\nu_k^p Q_{iky^p} + 4\nu_k^p Q_{iky^{p+1}})}{60(\nu_k^p (Q_{iky^p} + Q_{iky^{p+1}}) + \lambda_k^p)^2} \right] \quad (16)$$

The segment length (L^p) is given as $L^p = y^{p+1} - y^p$, where y^p and y^{p+1} are the left- and right-hand y -coordinates of the segment (for example, for a channel with n segments $y^1 = 0$ at the source end and $y^{n+1} = L$ at the drain end). In the above expressions, Q_{iky^p} and $Q_{iky^{p+1}}$ are the inversion charge densities at the left and right ends of the segment and can be given as

$$Q_{iky^p} = C_{oxk} (V_{gk} - \psi_k(y^p)) \quad (17)$$

$$Q_{iky^{p+1}} = C_{oxk} (V_{gk} - \psi_k(y^{p+1})) \quad (18)$$

$$\nu_1^p = \frac{1}{2} \left[\frac{1}{C_{ox1}} + \frac{(m_1^p)^2}{C_{ox2}} \right] \quad (19)$$

$$\nu_2^p = \frac{1}{2} \left[\frac{(m_2^p)^2}{C_{ox1}} + \frac{1}{C_{ox2}} \right] \quad (20)$$

$$\lambda_1^p = \frac{I_{ds}}{\mu \frac{W}{L} (Q_{i1y^p} - Q_{i1y^{p+1}})} - \nu_1^p (Q_{i1y^p} + Q_{i1y^{p+1}}) \quad (21)$$

$$\lambda_2^p = \frac{I_{ds}}{\mu \frac{W}{L} (Q_{i2y^p} - Q_{i2y^{p+1}})} - \nu_2^p (Q_{i2y^p} + Q_{i2y^{p+1}}) \quad (22)$$

where $m_1^p = (Q_{i2y^p} - Q_{i2y^{p+1}})/(Q_{i1y^p} - Q_{i1y^{p+1}})$ and $m_2^p = 1/m_1^p$. The total terminal charges can be obtained by simply adding up the respective terminal charges for each segment. There are three things to take note of as follows.

- 1) Each charge is divided into two components: Q^{plo} , which denotes the low V_{ds} component, and Q^{phi} , which denotes the high V_{ds} component. Q^{phi} becomes insignificant in comparison to Q^{plo} when V_{ds} is very low. As the formulation of Q^{plo} is source drain symmetric (can be also obtained by assuming the linear distribution of $\psi_{1(2)}$ with respect to y), the proposed model is symmetric around $V_{ds} = 0$ [14].
- 2) When there is no segment (i.e., $n = 0$), y^p in (12) becomes zero, and (11)–(16) becomes mathematically equivalent to the charge model proposed earlier [14].
- 3) The piecewise linearization technique might be applicable to other models [9]. However, the proposed model is “derivative free” and thus appears to be more numerically robust than the other model (that involves parameter

such as $\alpha' = d\theta/d\alpha$ [9], which is derived from the IVE. As the IVE has discontinuity/singularity, it is difficult to maintain the continuity of the derivative particularly around the $G = 0$ point).

In the proposed charge model, we basically divide a single MOSFET into several MOSFETs so that conventional charge linearization technique can be extended in the presence of nonlinearity between the surface potentials. As the terminal charges can be obtained by arithmetic operations on surface potentials and terminal voltages, it could be extended to small geometry devices by a bulk transistor modeling approach [8]. It should be also noted that the segmentation concept, which was earlier used in [16], is semiempirical in nature and not “derivative free.”

C. Selection of Break Points and Secondary IVE

The proposed charge model requires the surface potential values at the break points. This is the main departure from the compact models for a bulk or symmetric DG MOSFET, as there, the charge model is the function of source and drain end surface potentials and does not depend on the surface potential at any point in between the source and the drain. As the drain current is a function of ψ_1 , ψ_2 , and G , one can segment the channel on ψ_1 scale or on ψ_2 scale or on G scale. If we segment the channel on ψ_1 scale, at a breakpoint, we need to know the value of ψ_2 and G for a given value of ψ_1 and the gate voltages. This is difficult as the P-IVEs [11] were expressed in terms of ψ_1 only when $V_{g1} > V_{g2}$. The same argument is applicable if we segment the channel on ψ_2 scale. However, the exercise of finding the value of the surface potentials at the break points could be made much easier if we segment the channel on G scale. For a given value of G and gate voltages, the P-IVEs get simplified to the following implicit equations (which we call S-IVE):

$$\tilde{f}(x) \equiv x \ln(x) + ax^2 + bx + c = 0 \quad (23)$$

where

$$a = \frac{\beta\epsilon_{si}\sqrt{G}}{2C_{ox1} \sinh\left(\frac{\beta t_{si}\sqrt{G}}{2}\right)} \quad (24)$$

$$b = \sqrt{G} \coth\left(\frac{\beta t_{si}\sqrt{G}}{2}\right) \left[1 - \frac{\beta\epsilon_{si}}{2C_{ox1}}\right] - \frac{C_{ox2}}{\epsilon_{si}}(V_{g1} - V_{g2}) \quad (25)$$

$$c = - \left[\frac{\sqrt{G} \cosh^2\left(\frac{\beta t_{si}\sqrt{G}}{2}\right)}{\sinh\left(\frac{\beta t_{si}\sqrt{G}}{2}\right)} \pm \sqrt{G} \sinh\left(\frac{\beta t_{si}\sqrt{G}}{2}\right) \right] \quad (26)$$

$$x = \cosh\left(\frac{\beta t_{si}\sqrt{G}}{2}\right) + \frac{\sinh\left(\frac{\beta t_{si}\sqrt{G}}{2}\right)}{\sqrt{G}}(\xi_1) \quad (27)$$

where $\xi_1 = (C_{ox1}/\epsilon_{si})(V_{g1} - \psi_1)$. The above S-IVE is written for hyperbolic mode ($G > 0$) and valid for $V_{g1} > V_{g2}$. For trigonometric mode, one needs to replace a hyperbolic operator with a trigonometric operator and to use a negative sign in (26). For $V_{g2} > V_{g1}$ cases, V_{g1} and V_{g2} , C_{ox1} and C_{ox2} have to be swapped in (25), and ξ_1 has to be replaced with ξ_2 , where $\xi_2 =$

TABLE I
SUGGESTED POSITIONS FOR THE BREAK POINTS

Number of break-points (n)	1	2	3
Position of the Break point (χ_i)	$\chi_1 = 0.1$	$\chi_1 = 0.15$ $\chi_2 = 0.03$	$\chi_1 = 0.02$ $\chi_2 = 0.08$ $\chi_3 = 0.3$

$(C_{ox2}/\epsilon_{si})(V_{g2} - \psi_2)$. In S-IVE, we always use the absolute value of G . For a given value of G at any break point, a , b , and c are constant, and we need to solve the equation $\tilde{f}(x) = 0$ to find the value of $\xi_{1(2)}$. It is worth noting that both the trigonometric and hyperbolic P-IVEs have discontinuity at $G = 0$, and the trigonometric P-IVE has additional discontinuity at $(\theta_{1(2)} = \pi$ [11]) point. As a result of fixing G at a particular value, the hyperbolic S-IVE is now free from any discontinuity. The trigonometric S-IVE has now one singularity (instead of two) at $x = 0$ point, which is equivalent to $\theta_{1(2)} = \pi$ of P-IVE. The solution technique of S-IVE is much simpler than that of P-IVE [17], as discussed in the Appendix.

As the main objective of channel segmentation is to achieve a piecewise linear relationship between ψ_1 and ψ_2 , one can put a large number of equally spaced break points between G_s and G_d in order to achieve very high accuracy. However, the computational efficiency degrades with the increase in the number of break points. We found that, instead of placing the break points in regular interval, if we place them in some “selected” positions, high accuracy in terminal charges could be obtained with very few number of points. Those “selected” positions, which were heuristically found, are shown in Table I. G_i (the value of G at break point “ i ,” which can be 1, 2, or 3 for $n = 3$) is computed using the respective χ_i shown in Table I, as $G_i = G_s + (G_d - G_s) * \chi_i$. This way, the user can select the number of break points based on the accuracy required.

III. RESULTS AND DISCUSSION

We have validated the proposed charge model against numerical simulation (obtained by solving the terminal charge integrals numerically) and with TCAD data [18]. The modern compact models are implemented in a circuit simulator in a charge-based approach in order to satisfy the charge conservation. However, the charge models are conventionally verified in terms of transcapacitance values, as any error in terminal charge calculation is magnified due to the presence of the derivative term in transcapacitance expressions [9]. As shown in Fig. 2, the number of break points increase the accuracy of the transcapacitance values in TH state, where NLF is high. However, for HH state (low NLF case), the charge model without any break points also provides reasonable accuracy. In Fig. 3, we have validated our model for different devices for different bias conditions, which demonstrates the fact that the “selected” break points (given in Table I) are independent of device parameters and bias values. Although there are nine independent transcapacitance values, we validate our model only for C_{g2g1} and C_{g2d} , as these two transcapacitance values get maximally affected by the NLF . We assure that an accurate prediction of those two transcapacitance values automatically guarantees the good accuracy of other transcapacitance values.

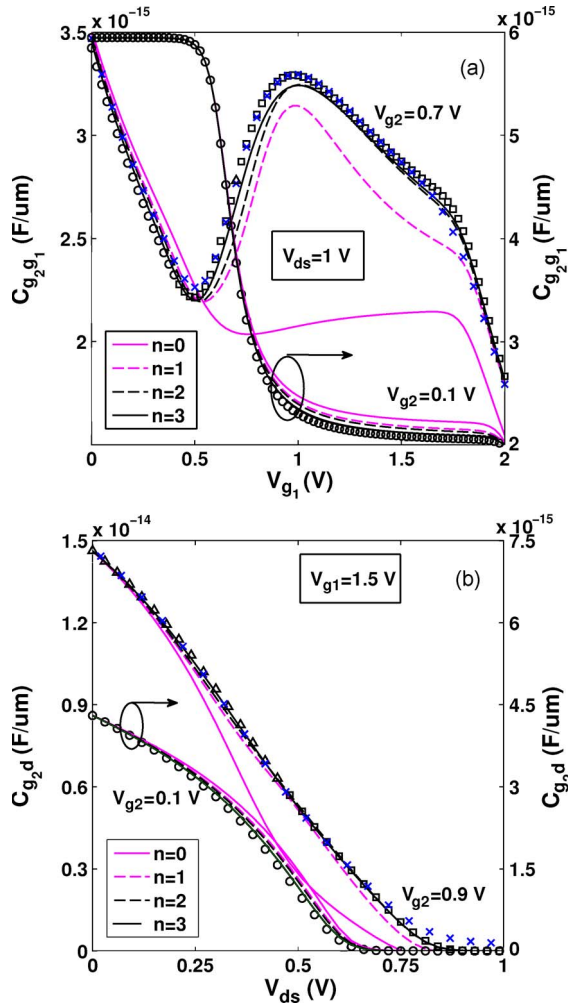


Fig. 2. Comparison of the transcapacitance (a) $C_{g_2g_1}$ and (b) C_{g_2d} characteristics predicted by the proposed model for different number of break points (lines) with the exact values obtained from numerical simulation. The types of symbols and the device parameters are the same as in Fig. 1. TCAD simulation data (crosses) are shown for few cases.

We implemented our model in a professional circuit simulator [19] through its Verilog-A interface. A 75-stage ring oscillator, an 8-bit ripple adder, and an 8-bit Johnson counter were successfully simulated using the proposed charge model. Two different circuit design approaches were adopted: (1) circuits using tied-gate configuration, where the transistor always operates in the trigonometric mode, and (2) circuits where the second gate is deactivated (grounded or connected to the source) so that the transistor operation is predominantly in the hyperbolic mode. Although for tied-gate configuration, the piecewise linearization technique is not required [14], we have used it to compare the simulation time between trigonometric and hyperbolic S-IVs. Table II depicts the simulation times observed for the mentioned circuits using different number of break points ($n = 1, 2, \text{ or } 3$) normalized with respect to the case where no-break point is used. One can find from Table II that the addition of each break points delays the simulation by an average 17% irrespective of the trigonometric or hyperbolic nature of S-IVE. Good convergence in all cases demonstrates practicality of the new charge model for the large-scale circuit simulation.

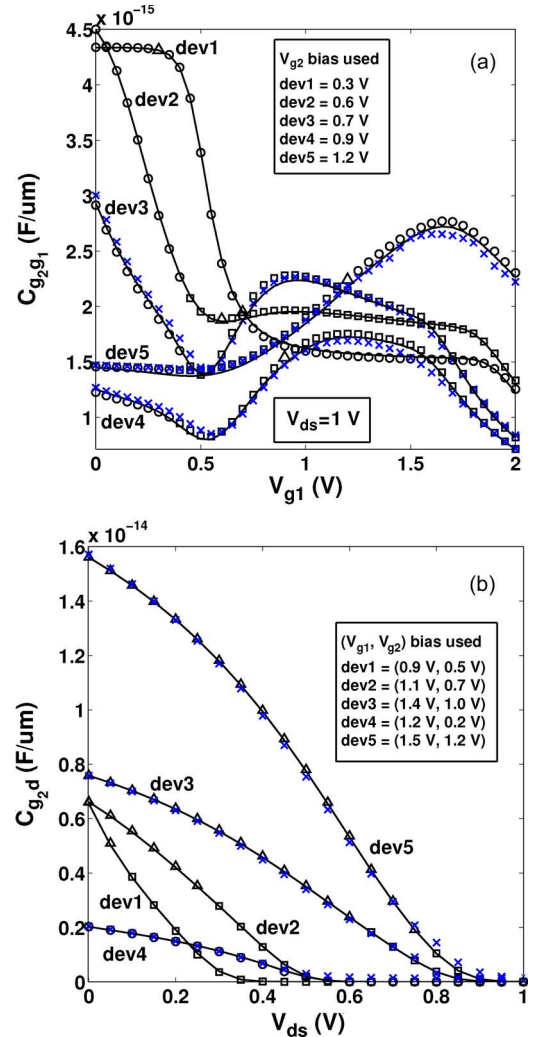


Fig. 3. Transcapacitance (a) $C_{g_2g_1}$ and (b) C_{g_2d} characteristics predicted by the proposed model for $n = 3$ for different devices (solid line) and the corresponding exact values obtained from numerical simulation (symbols as in Fig. 1) and TCAD simulation (crosses). Devices chosen are dev1: $t_{ox1} = 2$ nm, $t_{ox2} = 1$ nm, and $t_{si} = 15$ nm; dev2: $t_{ox1} = 2$ nm, $t_{ox2} = 2$ nm, and $t_{si} = 10$ nm; dev3: $t_{ox1} = 1$ nm, $t_{ox2} = 2$ nm, and $t_{si} = 15$ nm; dev4: $t_{ox1} = 2$ nm, $t_{ox2} = 3$ nm, and $t_{si} = 20$ nm; and dev5: $t_{ox1} = 4$ nm, $t_{ox2} = 1$ nm, and $t_{si} = 10$ nm. To keep the clarity of the figure, TCAD data have been put for few cases.

TABLE II
NORMALIZED SIMULATION TIME AS FOUND IN CIRCUIT SIMULATOR

Circuit	Tied-gate			Untied-Gate		
	n=1	n=2	n=3	n=1	n=2	n=3
75-stage Ring Oscillator	1.22	1.42	1.61	1.22	1.38	1.55
8-bit Adder	1.16	1.29	1.48	1.18	1.33	1.44
8-bit Counter	1.17	1.33	1.55	1.16	1.32	1.47

IV. CONCLUSION

We show that due to the nonlinear relationship that might prevail between the surface potentials of an IDG MOSFET, the position along the channel cannot be approximated as a quadratic function of the surface potential, which is a common practice in compact modeling of bulk and symmetric double-gate devices. We propose a new charge model, which takes into account this nonlinearity by a novel piecewise linearization technique. The proposed model is successfully implemented in a professional circuit simulator and found to be in good

agreement with numerical results and TCAD data for all bias conditions.

APPENDIX

Solution Techniques for S-IVEs: We solve the S-IVEs by Halley's method with optimized physics-based initial guesses, which are explained below for the $V_{g1} > V_{g2}$ case. When the S-IVE is hyperbolic in nature, then $\xi_2 \simeq \sqrt{G}$. Assuming a linear relationship between ξ_1 and ξ_2 along the channel, ξ_1 can be approximated as $\xi_1 \simeq [(\xi_{1s} - \xi_{1d})/(\xi_{2s} - \xi_{2d})]\xi_2 + (\xi_{2s}\xi_{1d} - \xi_{2d}\xi_{1s})/(\xi_{2s} - \xi_{2d})$. We use this approximate value of ξ_1 as an initial guess to solve the hyperbolic S-IVE.

When the S-IVE is trigonometric in nature, the equation has singularity, and thus, the solution space is bounded between $\xi_{1\min}$ and $\xi_{1\max}$, where $\xi_{1\max} = \xi_{1s}$ and $\xi_{1\min} = \max[\xi_{1d}, -\sqrt{G} \cot(\beta t_{si} \sqrt{G}/2)]$. (We always use an absolute value of G in the S-IVE expression.) Now, we use $(\xi_{1\min} + \xi_{1\max})/2$ as an initial guess for the Halley's method to solve the S-IVE. However, in the presence of singularity, a derivative-based root finding method (e.g., Halley) cannot assure convergence. Hence, we use LZ4 [17], [20] as a backup. During iteration in Halley's loop, if the root goes out of the solution space, we switch to LZ4 in order to achieve assured convergence.

REFERENCES

- [1] H. M. Shrivastava, M. S. Baghini, A. B. Sachid, D. K. Sharma, and V. R. Rao, "A novel and robust approach for common mode feedback using IDDG FinFET," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3274–3282, Nov. 2008.
- [2] M.-H. Chiang, K. Kim, C.-T. Chuang, and C. Tretz, "High-density reduced-stack logic circuit techniques using independent-gate controlled double-gate devices," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2370–2377, Sep. 2006.
- [3] S. A. Tawfik and V. Kursun, "Low-power and compact sequential circuits with independent-gate FinFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 60–70, Jan. 2008.
- [4] A. Amara and O. Rozeau, *Planar Double-Gate Transistor: From Technology to Circuit*. New York: Springer-Verlag, 2009.
- [5] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling*. Hoboken, NJ: Wiley, 2006.
- [6] G. Gildenblat, *Compact Modeling: Principles, Techniques and Applications*. New York: Springer-Verlag, 2010.
- [7] J. M. Sallese, F. Krummenacher, F. Pregaldiny, C. Lallement, A. Roy, and C. Enz, "A design oriented charge-based current model for symmetric DG MOSFET and its correlation with the EKV formalism," *Solid State Electron.*, vol. 49, no. 3, pp. 485–489, Mar. 2005.
- [8] G. Dessai, A. Dey, G. Gildenblat, and G. D. J. Smit, "Symmetric linearization method for double-gate and surrounding-gate MOSFET model," *Solid State Electron.*, vol. 53, no. 5, pp. 548–556, May 2009.
- [9] G. Dessai, W. Wu, and G. Gildenblat, "Compact charge model for independent-gate asymmetric DGFET," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2106–2115, Sep. 2010.
- [10] F. Liu, J. He, Y. Fu, J. Hu, W. Bian, Y. Song, X. Zhang, and M. Chan, "Generic carrier-based core model for undoped four-terminal double-gate MOSFETs valid for symmetric, asymmetric, and independent-gate-operation modes," *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 816–826, Mar. 2008.
- [11] A. Sahoo, P. K. Thakur, and S. Mahapatra, "A computationally efficient generalized Poisson solution for independent double gate transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 3, pp. 632–636, Mar. 2010.
- [12] Y. Tsvetkov and C. McAndrew, *Operation and Modeling of the MOS Transistor*. London, U.K.: Oxford Univ. Press, 2010.
- [13] D. E. Ward and R. W. Dutton, "A charge-oriented model for MOS transistor capacitances," *IEEE J. Solid-State Circuits*, vol. SC-13, no. 5, pp. 703–708, Oct. 1978.
- [14] S. Jandhyala, R. Kashyap, C. Anghel, and S. Mahapatra, "A simple charge model for symmetric double-gate MOSFETs adapted to gate-oxide-thickness asymmetry," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1002–1007, Apr. 2012.
- [15] K. Emanipator and M. K. Kroll, "A quantitative measure of nonlinearity," *Clin. Chem.*, vol. 39, no. 5, pp. 766–772, 1993.
- [16] P. K. Thakur and S. Mahapatra, "Large signal model for independent DG MOSFET," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 46–52, Jan. 2011.
- [17] A. Abraham, S. Jandhyala, and S. Mahapatra, "Improvements in efficiency of surface potential computation for independent DG MOSFET," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1199–1202, Apr. 2012.
- [18] ATLAS Device Simulation Framework—Users' Manual, Version 5.17.18.c, Silvaco Int., Santa Clara, CA, 2010. [Online]. Available: www.silvaco.com
- [19] Smartspice, Analog Circuit Simulator—Users' Manual, Version 4.3.2, Silvaco Int., Santa Clara, CA, 2010. [Online]. Available: www.silvaco.com
- [20] D. Le, "An efficient derivative-free method for solving nonlinear equations," *ACM Trans. Math. Softw.*, vol. 11, no. 3, pp. 250–262, Sep. 1985.



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