

Modeling of Channel Potential and Subthreshold Slope of Symmetric Double-Gate Transistor

Biswajit Ray and Santanu Mahapatra, *Member, IEEE*

Abstract—A new physically based classical continuous potential distribution model, particularly considering the channel center, is proposed for a short-channel undoped body symmetrical double-gate transistor. It involves a novel technique for solving the 2-D nonlinear Poisson's equation in a rectangular coordinate system, which makes the model valid from weak to strong inversion regimes and from the channel center to the surface. We demonstrated, using the proposed model, that the channel potential versus gate voltage characteristics for the devices having equal channel lengths but different thicknesses pass through a single common point (termed “crossover point”). Based on the potential model, a new compact model for the subthreshold swing is formulated. It is shown that for the devices having very high short-channel effects (SCE), the effective subthreshold slope factor is mainly dictated by the potential close to the channel center rather than the surface. SCEs and drain-induced barrier lowering are also assessed using the proposed model and validated against a professional numerical device simulator.

Index Terms—Compact model, device simulator, double-gate (DG) Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET), Poisson's equation, short-channel effect (SCE), subthreshold slope.

I. INTRODUCTION

THE DOUBLE-GATE (DG) Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) is appearing as a replacement for the single gate bulk MOSFET in forthcoming sub-45-nm technology nodes. As in the DG MOSFET, the short-channel effect (SCE) is controlled by the device geometry, an undoped (or, lightly doped) body is used to sustain the channel. The undoped channel also helps to alleviate several other problems related to nanoscale MOSFETs, e.g., mobility degradation, random dopant fluctuations, compatibility with midgap metal gate, etc. In bulk transistor, where the substrate is sufficiently doped, the inversion charges are located close to the surface, and hence, the surface potential solely controls the electrostatic integrity of the device. However, in undoped body

Manuscript received August 18, 2008; revised November 7, 2008. Current version published January 28, 2009. This work was supported by the Department of Science and Technology (DST), India, under Grant SR/FTP/ETA-05/2006. The review of this paper was arranged by Editor C. McAndrew.

B. Ray was with the Nano Scale Device Research Laboratory, Centre for Electronics Design and Technology, Indian Institute of Science, Bangalore 560 012, India. He is now with Electrical and Communication Department, Purdue University, West Lafayette, IN 47907 USA (e-mail: ray0@purdue.edu).

S. Mahapatra is with the Nano Scale Device Research Laboratory, Centre for Electronics Design and Technology, Indian Institute of Science, Bangalore 560 012, India (e-mail: santanu@cedt.iisc.ernet.in).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TED.2008.2010577

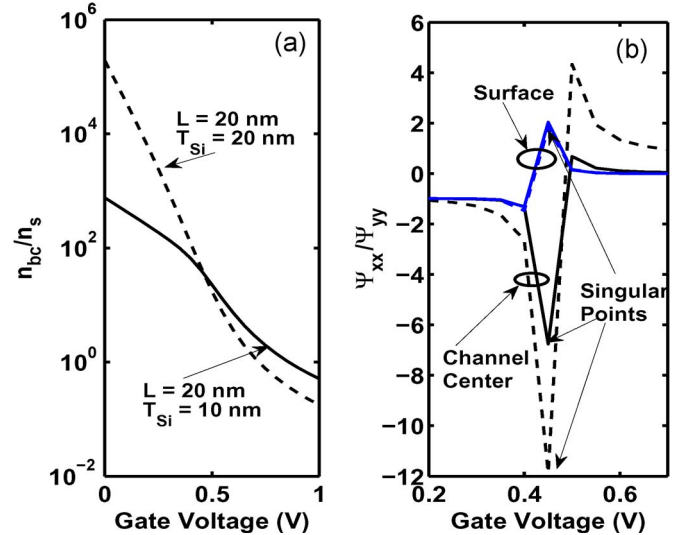


Fig. 1. (a) Ratio of carrier concentration at body center (n_{bc}) and surface (n_s) as a function of gate voltage. (b) Ratio of the horizontal (Ψ_{xx}) and vertical component (Ψ_{yy}) of the Poisson equation as a function of gate voltage. Here, L and T_{Si} are the body length and thickness.

devices, the gate electric field penetrates the channel center, and the inversion charge exists throughout the channel. In contrast to bulk transistors, depending on device geometry, the potential of the channel center of undoped body devices could be higher than the surface in a weak inversion regime, and the current flows through the center-part of the device instead of the surface [see Fig. 1(a)]. Several crucial parameters (e.g., subthreshold slope) sometimes become more dependable on the potential of the channel center rather than the surface. Hence, the channel-center potential should also be modeled correctly along with the surface-potential for the accurate calculation of subthreshold phenomena.

Several potential models for DG transistors have been proposed [1]–[6] to capture the short-channel behavior in the subthreshold regime. Some of them [2] are based on the crucial approximation of converting the 2-D nonlinear Poisson's equation into the 2-D Laplace's equation, and many of them [1], [4] are based on the approximation of converting the 2-D nonlinear Poisson's equation into a summation of the 1-D Poisson's and the 2-D Laplace's equation. From Fig. 1(b), one can see that the Laplace approximation is valid only at the surface region as the ratio between the horizontal and vertical components of Poisson's equation is close to -1 (i.e., $\nabla^2\Psi = 0$) but deviates significantly at the channel center region. This deviation gets magnified for devices having a smaller L and higher T_{Si}/L ratio. Moreover, the Laplace approximation is not

at all valid in moderate inversion regimes at the surface and body center. As a result, most of the previous models fail to capture the potential of the body center correctly for devices having ultrasmall channel lengths and high T_{Si}/L ratios and also remain valid only in a weak inversion regime.

In this paper, we propose a new technique for solving the 2-D nonlinear Poisson's equation for modeling the DG transistor channel potential. The proposed model is much more accurate than the previous models and is capable of predicting the potential at any point of the channel with excellent accuracy in both weak and strong inversion regimes. Using the potential model, we demonstrate that the channel potential versus gate voltage characteristics for devices having equal channel lengths but different thicknesses pass through a single common point, which is termed the "crossover point." Based on the potential model, a new model for the subthreshold slope is also formulated. Some other parameters, e.g., SCE and DIBL (drain-induced barrier lowering) are also computed and compared with a professional numerical device simulator.

II. MODEL DERIVATION

Fig. 2 shows the 2-D structural view of the DG MOS considered in this paper. On the assumption that the channel is undoped and has a larger thickness (> 5 nm) to ignore energy quantization, the electrostatics of the channel region is solely governed by the following nonlinear Poisson's equation, with only the mobile charge term included:

$$\nabla^2 \Psi(x, y) = \frac{q}{\epsilon_{Si}} n_i e^{(\Psi(x, y) - \Psi_F(x))/U_T} \quad (1)$$

with boundary conditions

$$\Psi(0, y) = V_{bi} \quad (2)$$

$$\Psi(L, y) = V_{bi} + V_{ds} \quad (3)$$

$$\left. \frac{\partial \Psi}{\partial y} \right|_{y=\frac{T_{Si}}{2}} = \frac{C_{ox}}{\epsilon_{Si}} \left(V_{gs} - \Phi_{ms} - \Psi \left(\frac{T_{Si}}{2} \right) \right) \quad (4)$$

$$\left. \frac{\partial \Psi}{\partial y} \right|_{y=0} = 0 \quad (5)$$

where $\Psi(x, y)$ is the potential at the point (x, y) , q is the electronic charge, n_i is the intrinsic electron density in Silicon, U_T is the thermal voltage, Φ_{ms} is the gate workfunction referenced to intrinsic Silicon, V_{bi} is the $n^+ - i$ diode's built-in potential, C_{ox} is the gate oxide capacitance ($C_{ox} = \epsilon_{ox}/T_{ox}$), T_{ox} is the gate oxide thickness, ϵ_{ox} and ϵ_{Si} are the permittivity of gate oxide and silicon, respectively, V_{gs} and V_{ds} are the applied gate voltage and drain voltage, and $\Psi_F(x)$ is the electron quasi-fermi level whose value at the source end is taken as the reference potential. It is worth noting that here, we have ignored the hole concentration, and thus, the model is only valid for $\Psi > 3U_T$, where the hole concentration will be very low compared to the electron concentration.

As (1) is a nonlinear partial differential equation (PDE), it is very difficult to obtain a computationally efficient analytical solution for it. In this paper, we have taken a few assump-

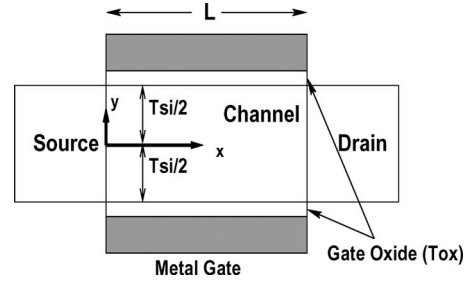


Fig. 2. Schematic of a DG MOSFET.

tions to obtain such a solution. First, we assume $\Psi(x, y) = \Psi_0(y) + \Psi_1(x, y)$, where $\Psi_0(y)$ and $\Psi_1(x, y)$ are defined by the following DEs:

$$\nabla^2 \Psi_0(y) = \frac{q}{\epsilon_{Si}} n_i e^{\Psi_0/U_T} \quad (6)$$

with boundary conditions

$$\epsilon_{Si} \left. \frac{\partial \Psi_0}{\partial y} \right|_{y=\frac{T_{Si}}{2}} = C_{ox} \left(V_{gs} - \Phi_{ms} - \Psi_0 \left(\frac{T_{Si}}{2} \right) \right) \quad (7)$$

$$\left. \frac{\partial \Psi_0}{\partial y} \right|_{y=0} = 0 \quad (8)$$

and

$$\nabla^2 \Psi_1(x, y) = \frac{q}{\epsilon_{Si}} n_i e^{\Psi_0/U_T} \left(e^{\Psi_1/U_T} - 1 \right) \quad (9)$$

with boundary conditions

$$\Psi_1(0, y) = V_{bi} - \Psi_0(y) \quad (10)$$

$$\Psi_1(L, y) = V_{bi} + V_{ds} - \Psi_0(y) \quad (11)$$

$$\left. \frac{\partial \Psi_1}{\partial y} \right|_{y=\frac{T_{Si}}{2}} = - \frac{C_{ox}}{\epsilon_{Si}} \Psi_1 \left(\frac{T_{Si}}{2} \right) \quad (12)$$

$$\left. \frac{\partial \Psi_1}{\partial y} \right|_{y=0} = 0. \quad (13)$$

Since the main Poisson's equation (1) is nonlinear, the aforementioned assumption is mathematically questionable. However, the device physics supports it as we split the total potential $\Psi(x, y)$ into long channel ($\Psi_0(y)$) and short-channel ($\Psi_1(x, y)$) components so that $\Psi_1 \rightarrow 0$ as $L \rightarrow \infty$. Now, the solution of (9) is also not a straightforward one. Previous authors [1], [4] have solved this PDE by approximating it as the Laplace equation (i.e., $\nabla^2 \Psi_1(x, y) = 0$). However, as described in Section I, such approximation cannot predict the channel center potential accurately for devices having small channel lengths and high T_{Si}/L ratios. In order to obtain more accurate solution, in this paper, we split Ψ_1 further as $\Psi_1(x, y) = \Psi_L(y) + \Psi_N(x, y)$. Here, $\Psi_L(x, y)$ is the Laplace part including all the boundary conditions, and $\Psi_N(x, y)$ is the remaining nonlinear part with all boundary conditions set to zero

$$\nabla^2 \Psi_L(x, y) = 0 \quad (14)$$

with boundary conditions

$$\Psi_L(0, y) = V_{bi} - \Psi_0(y) \quad (15)$$

$$\Psi_L(L, y) = V_{bi} + V_{ds} - \Psi_0(y) \quad (16)$$

$$\epsilon_{Si} \frac{\partial \Psi_L}{\partial y} \Big|_{y=\frac{T_{Si}}{2}} = -C_{ox} \Psi_L \left(\frac{T_{Si}}{2} \right) \quad (17)$$

$$\frac{\partial \Psi_L}{\partial y} \Big|_{y=0} = 0 \quad (18)$$

and

$$\nabla^2 \Psi_N(x, y) = \frac{q}{\epsilon_{Si}} n_i e^{\Psi_0/U_T} \left(e^{(\Psi_L + \Psi_N - \Psi_F)/U_T} - 1 \right) \quad (19)$$

with boundary conditions

$$\Psi_N(0, y) = 0 \quad (20)$$

$$\Psi_N(L, y) = 0 \quad (21)$$

$$\epsilon_{Si} \frac{\partial \Psi_N}{\partial y} \Big|_{y=\frac{T_{Si}}{2}} = -C_{ox} \Psi_N \left(\frac{T_{Si}}{2} \right) \quad (22)$$

$$\frac{\partial \Psi_N}{\partial y} \Big|_{y=0} = 0. \quad (23)$$

Equation (6) is an ordinary differential equation whose solution is given below [7]

$$\Psi_0(y) = U_T \ln \left[\left(\frac{2L_D \beta}{T_{Si}} \right)^2 \sec^2 \left(\frac{2\beta y}{T_{Si}} \right) \right]. \quad (24)$$

Here, β is a parameter whose value depends on V_{gs} as follows:

$$\ln(\beta) - \ln(\cos \beta) + r\beta \tan \beta - F = 0 \quad (25)$$

where

$$r = \frac{2\epsilon_{Si} T_{ox}}{\epsilon_{ox} T_{Si}} \quad (26)$$

$$F = \frac{V_{gs}}{2U_T} - \ln \left(\frac{2L_D}{T_{Si}} \right) \quad (27)$$

$$L_D = \sqrt{\frac{2\epsilon_{Si} U_T}{qn_i}}. \quad (28)$$

Although the expression of β (25) is implicit, it can be calculated explicitly with high accuracy as shown in [7].

Equation (14) is a mixed boundary value problem which can be solved by the variable separation method. As a similar problem has been solved in several articles [1], [2], [4], the final solution is given below without any derivation

$$\Psi_L(x, y) = \sum_{n=1}^{\infty} \left[A_n \sinh \left(\frac{2\mu_n x}{T_{Si}} \right) + B_n \sinh \left(\frac{2\mu_n (L-x)}{T_{Si}} \right) \right] \times \cos \left(\frac{2\mu_n y}{T_{Si}} \right) \quad (29)$$

where A_n, B_n are formulated as

$$A_n = \frac{4 \int_0^{\frac{T_{Si}}{2}} (V_{bi} + V_{ds} - \Psi_0(y)) \cos \left(\frac{2\mu_n y}{T_{Si}} \right) dy}{T_{Si} \sinh \left(\frac{2\mu_n L}{T_{Si}} \right) \left(\frac{2\epsilon_{Si} \sin^2(\mu_n)}{C_{ox} T_{Si}} + 1 \right)} \approx \frac{2 \left(V_{bi} + V_{ds} - 2U_T \ln \left(\frac{2L_D \beta}{T_{Si}} \right) \right) \sin(\mu_n)}{\mu_n \sinh \left(\frac{2\mu_n L}{T_{Si}} \right) \left(\frac{2\epsilon_{Si} \sin^2(\mu_n)}{C_{ox} T_{Si}} + 1 \right)} \quad (30)$$

$$B_n = \frac{4 \int_0^{\frac{T_{Si}}{2}} (V_{bi} - \Psi_0(y)) \cos \left(\frac{2\mu_n y}{T_{Si}} \right) dy}{T_{Si} \sinh \left(\frac{2\mu_n L}{T_{Si}} \right) \left(\frac{2\epsilon_{Si} \sin^2(\mu_n)}{C_{ox} T_{Si}} + 1 \right)} \approx \frac{2 \left(V_{bi} - 2U_T \ln \left(\frac{2L_D \beta}{T_{Si}} \right) \right) \sin(\mu_n)}{\mu_n \sinh \left(\frac{2\mu_n L}{T_{Si}} \right) \left(\frac{2\epsilon_{Si} \sin^2(\mu_n)}{C_{ox} T_{Si}} + 1 \right)}. \quad (31)$$

The eigenvalue μ_n can be found from the following relation which gives infinitely possible values of μ :

$$\mu_n \tan(\mu_n) = \frac{C_{ox} T_{Si}}{2\epsilon_{Si}}. \quad (32)$$

Although the expression of $\Psi_L(x, y)$ consists of an infinite number of terms, it is found that the higher order ($n > 3$) terms vanish very rapidly.

Equation (19) is a nonlinear second order PDE which is solved in the neighborhood of the boundary $y = 0$ (see the Appendix). The final solution can be formulated as

$$\Psi_N(x, y) = (\Psi_{L0}(x, y) - V_0) \left(\frac{\cosh \left\{ P \left(\frac{L}{2} - x \right) \right\}}{\cosh \left(\frac{PL}{2} \right)} - 1 \right) \quad (33)$$

where Ψ_{L0} is the value of Ψ_L evaluated at $V_{ds} = 0$ and P, V_0 are functions of y as given below

$$P = \sqrt{\frac{qn_i}{\epsilon_{Si} U_T}} e^{\frac{\Psi_0(y)}{2U_T}} \quad (34)$$

$$V_0 = U_T \left[1 + \frac{\Psi_{L0} \left(\frac{L}{2}, y \right) + \Psi_N \left(\frac{L}{2}, y \right)}{U_T} - \exp \left(\left(\Psi_{L0} \left(\frac{L}{2}, y \right) + \Psi_N \left(\frac{L}{2}, y \right) \right) / U_T \right) \right]. \quad (35)$$

In the expression of Ψ_N, V_0 first has to be calculated from (33) at $x = L/2$. We solve the resulting equation for $\Psi_N((L/2), y)$ by Halley's method [8]. By simulation, we observe that the value of $\Psi_N((L/2), y)$ lies in the range 0 to $-3U_T$, and hence, we take the initial guess for the iteration as $-U_T$ which gives excellent accuracy in the first iteration itself. The final expression for $\Psi_N((L/2), y)$ obtained by Halley's method is given below

$$\Psi_N \left(\frac{L}{2}, y \right) \approx \Psi_{N0} - \left(1 + \frac{1}{2} \frac{L_f(\Psi_{N0})}{1 - \frac{1}{2} L_f(\Psi_{N0})} \right) \frac{f(\Psi_{N0})}{f'(\Psi_{N0})} \quad (36)$$

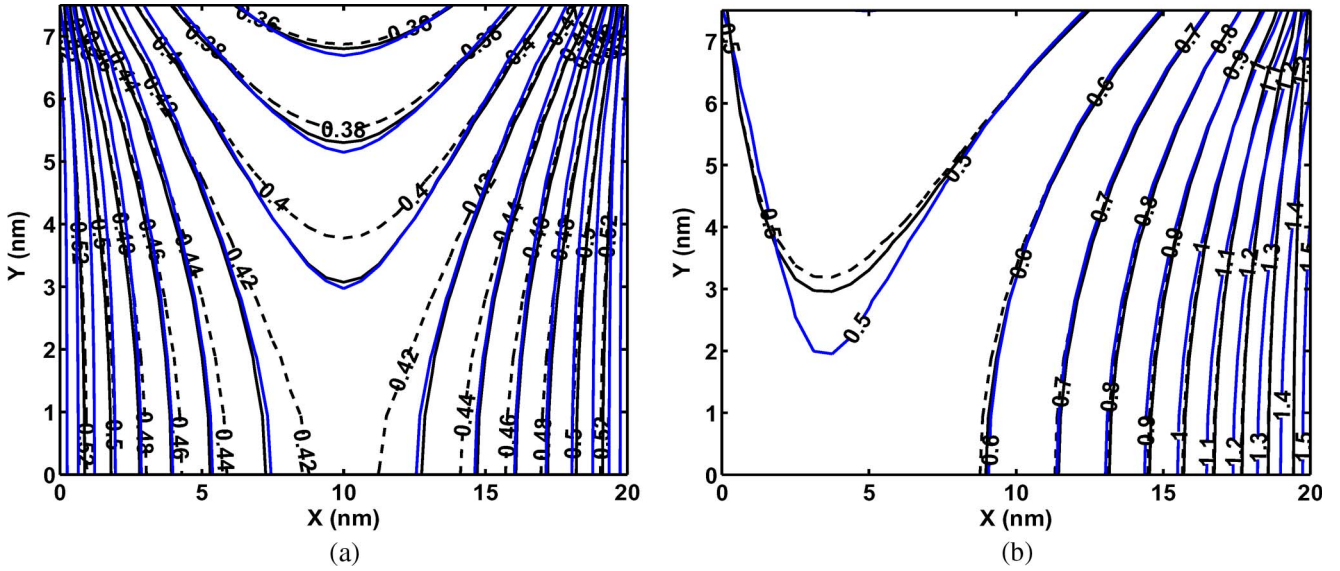


Fig. 3. Constant electrostatic potential contours. Blue solid lines represents the simulation curves, the black solid lines are for the model with Ψ_N part, and the dashed lines are for model without Ψ_N . Here, $L = 20$ nm, $T_{Si} = 15$ nm, and $V_{gs} = 0.3$ V. (a) $V_{ds} = 0$ V. (b) $V_{ds} = 1$ V.

where

$$L_f(\Psi_{N0}) = \frac{f''(\Psi_{N0})f(\Psi_{N0})}{f'(\Psi_{N0})^2} \quad (37)$$

$$f(\Psi_N) = \Psi_N - U_T \left(1 - \cosh\left(\frac{PL}{2}\right) \right) \left(e^{\frac{\Psi_{L0} + \Psi_N}{U_T}} - 1 \right) \quad (38)$$

where $\Psi_{N0} (= -U_T)$ is the initial guess.

The Ψ_N component takes care of the inversion charge, which is generated due to a lateral electric field under a high SCE condition and could be treated as a correction term over previous works [1], [4]. The contribution of Ψ_N will only be visible at low V_{ds} for devices having very small channel lengths (< 50 nm) and high T_{Si}/L ratios (> 0.4). Due to the same reason, Ψ_N is more useful for channel center potential modeling than the surface. The approximation of the Fermi level (45) becomes very crucial for the calculation of Ψ_N for high V_{ds} . Without the knowledge of $\Psi_F(x)$ (which can only be obtained by solving the carrier continuity equation), at high V_{ds} , it is difficult to obtain a good solution for Ψ_N due to the high discontinuity of $d\Psi/dy$ at $(L, (T_{Si}/2))$. As a result, the contribution of Ψ_N will not be significant at high V_{ds} . In the subsequent sections, we will show that if Ψ_N is ignored, the model: 1) predicts the surface potential quite accurately in weak inversion but overpredicts it in the strong and moderate inversion region; 2) predicts the channel center potential quite inaccurately both in the weak and strong inversions; and 3) does not show any ‘‘crossover point.’’

III. RESULTS AND DISCUSSION

A. Model Verification

The proposed potential model is verified against the data obtained from the numerical device simulator Atlas [9] for different device geometries. Fig. 3 shows the potential distri-

bution over the X – Y plane for $V_{ds} = 0$ V and 1 V, as the expected contribution of Ψ_N is more visible for $V_{ds} = 0$ V. From Fig. 4(a)–(d), one can observe that the proposed model predicts the surface as well as the channel center potential quite accurately both in the subthreshold and strong inversion regions. It can also be observed [from Fig. 4(e)] that without the Ψ_N component (which is equivalent to the previous model [1]), there is a significant mismatch between simulation and model predicted results for the channel center potential. This mismatch increases with the increasing value of the T_{Si}/L ratio, which leads to higher SCEs.

B. Crossover Point

Another important observation made in this paper is ‘‘crossover point.’’ From Fig. 4(e), we note that the potential at the surface, channel center, and at $y = T_{Si}/4$ crosses through a common point for a particular gate voltage (V_{FB}). This implies that at V_{FB} , there is no potential drop along the vertical direction from the channel center to the surface. This is precisely the flatband condition. However, we call this situation a ‘‘Pseudo Flat Band condition’’ because there exists a potential variation along the lateral direction. Interestingly, it is also observed that [inset of Fig. 4(f)] V_{FB} is *almost* independent of the variation of channel thickness when the channel length is constant, or in other words, devices having the same L but different T_{Si} hold *almost* the same value of V_{FB} . Hence, for a given L and different T_{Si} s, if we plot the potential as a function of V_{gs} at a particular point $(L/2, (T_{Si} \cdot m))$, where $|m| (< 1/2)$ is a constant, all the characteristics should pass through the common ‘‘pseudo flatband’’ point, which we termed a ‘‘crossover point’’ [Fig. 4(a) and (b)]. The body potential related to this point is denoted by Ψ_{cross} . From Fig. 4(e), we see that the previous model predicts the V_{FB} incorrectly, and thus, it also fails to predict the ‘‘crossover point’’ [Fig. 4(b)]. One more observation made in this paper is that the value of Ψ_{cross} increases with decreasing channel length, as shown in

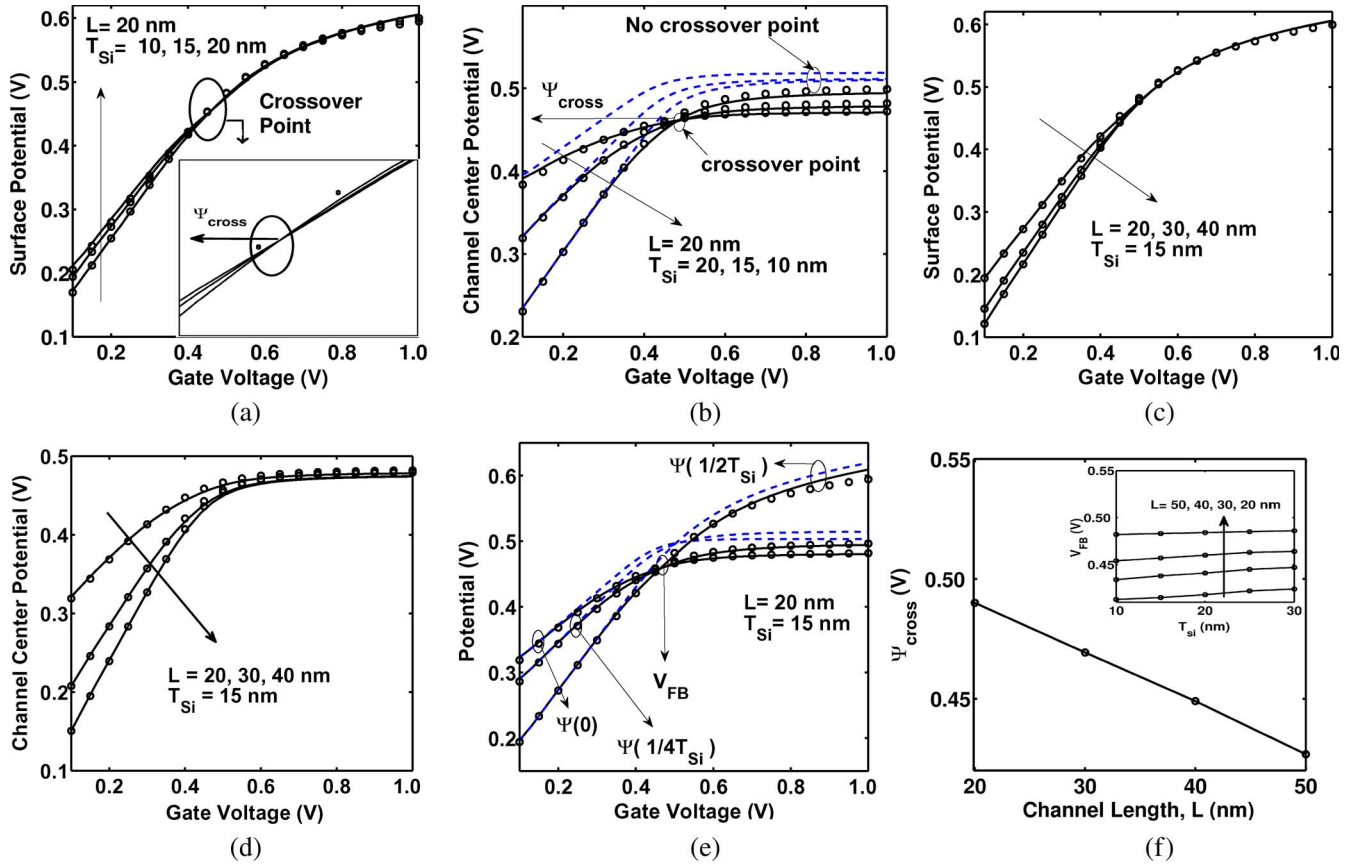


Fig. 4. Validation of (solid curves) the analytical model with (symbols) the numerical simulation results obtained from the Atlas Device Simulator. (a) Surface potential (Ψ_s) versus gate voltage (V_{gs}) @ $x = L/2$ for a fixed channel length $L = 20$ nm. (b) Channel center potential (Ψ_b) versus gate voltage (V_{gs}) @ $x = L/2$ for a fixed channel length $L = 20$ nm. The same has been shown as a series of dashes without considering the Ψ_N part. (c) Surface potential versus gate voltage for a fixed channel thickness $T_{Si} = 15$ nm. (d) Channel center potential versus gate voltage @ $x = L/2$ for a fixed channel thickness $T_{Si} = 15$ nm. (e) Ψ_s , Ψ_b , and $\Psi(y = T_{Si}/4)$ @ $x = L/2$ calculated (solid lines) considering the $\Psi_N(x, y)$ term, and (dashed lines) not considering the $\Psi_N(x, y)$ term. (f) Change of Ψ_{cross} as a function of L . The inset shows V_{FB} as a function of T_{Si} . In all the cases $V_{ds} = 0$ V and $T_{ox} = 1$ nm, midgap gate metal is used.

Fig. 4(f). This is due to the fact that for long-channel devices $\Psi \sim \Psi_0$, and for positive V_{gs} (more precisely for $V_{gs} > \Phi_{ms}$) $\Psi_0(T_{Si}/2) > \Psi_0(0)$. Hence, for long-channel devices, $V_{FB} \approx 0$ (or Φ_{ms}). However, for short-channel devices, because of the contribution of Ψ_L and Ψ_N , $\Psi(T_{Si}/2)$ could be less than $\Psi(0)$ for positive V_{gs} . Hence, in order to make the $\Psi(T_{Si}/2)$ equal to $\Psi(0)$, one needs a higher gate voltage. As a result, Ψ_{cross} increases with decreasing L .

C. SCE and DIBL

The inversion charge (in coulombs per square meter) at $x = (L/2)$ can be calculated from the potential model as shown below

$$Q = qn_i \int_0^{T_{Si}/2} e^{\Psi(L/2, y)/U_T} dy. \quad (39)$$

We have used the proposed potential model and have calculated SCE and DIBL and compared them with a numerical device simulation. Threshold voltages for different device geometries are first extracted from the I_d - V_{gs} plot (obtained from the Atlas simulation) using the Match Point method [10]. The threshold voltage is then calculated from the potential model by using the

criteria $Q = Q_{TH}$, where Q_{TH} is the threshold charge. $Q_{TH} = 1 \times 10^{-4}$ C/m² is taken in order to obtain the best match with the values extracted from the Atlas simulation. The threshold voltage roll-off is shown in Fig. 5. As expected, the contribution of Ψ_N is more evident in the SCE plot than the DIBL. It is also observed that the difference between the two models (with and without Ψ_N) decreases with decreasing SCE. It should be noted that for DIBL, (39) is calculated at $x = X_c$, where X_c is the virtual cathode defined as $(d\Psi(x, 0)/dx)|_{x=X_c} = 0$.

D. Modeling of Subthreshold Slope

The subthreshold slope (S) is defined as

$$S = 2.3U_T\eta(y_{eff}) \quad (40)$$

where η is known as the subthreshold slope factor. For bulk devices, η is calculated from the inverse slope of the surface potential versus gate voltage characteristics. However, it is not so straightforward in the case of undoped body devices. As observed from Figs. 1(a) and 4(e), the channel center potential could be greater than the surface, and thus, the central part of the body provides the most leaky path for subthreshold current conduction. In Table I, η_{I-V} represents the actual subthreshold slope factor extracted from I_d - V_{gs} plot (obtained from the Atlas

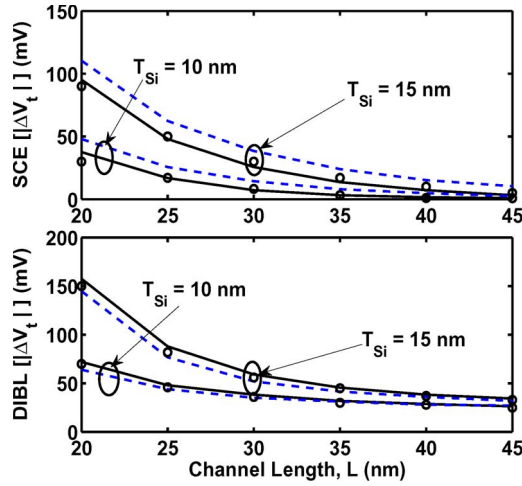


Fig. 5. SCE and DIBL plotted as a function of channel length. The symbols represent data extracted from Atlas I_d-V_{gs} characteristics, solid lines are for the model including Ψ_N , and the dashes are for the model excluding Ψ_N .

TABLE I
SUBTHRESHOLD SLOPE FACTOR

L (nm)	T_{Si} (nm)	η_{I-V}	η_s	η_b
20	10	1.37	1.17	1.37
	15	1.92	1.26	1.93
	20	2.97	1.32	3.00
25	10	1.21	1.10	1.21
	15	1.50	1.17	1.51
	20	2.00	1.22	2.02
30	10	1.12	1.06	1.12
	15	1.30	1.11	1.30
	20	1.60	1.15	1.61

device simulator), and η_b and η_s represent the slope factor value calculated from the $\Psi(L/2, 0) - V_{gs}$ and $\Psi(L/2, T_{Si}/2) - V_{gs}$ characteristics, respectively. It can be seen from this table that for undoped body devices, η is a function of y , and the effective subthreshold slope factor could be denoted as $\eta(y_{eff})$, where y_{eff} represents the position of the effective conducting path for subthreshold current [11].

As a first-order approximation, $y_{eff} = (T_{Si}/16)$ is taken in this paper, and for this assumption, we get an excellent match with the Atlas results, as shown in Fig. 6. The expression for S , which is derived from the potential model, is given as

$$S = 2.3U_T\eta(y_{eff}) = 2.3U_T \left[\frac{\partial\Psi(x, y)}{\partial V_g} \right]^{-1} \Bigg|_{x=L/2, y=y_{eff}} \quad (41)$$

where

$$\frac{\partial\Psi(x, y)}{\partial V_g} = \left[1 + \alpha + \frac{\alpha \left(1 - \cosh\left(\frac{PL}{2}\right) \right) + \left(1 - e^{-\frac{\Psi_L + \Psi_N}{U_T}} \right)}{e^{-\frac{\Psi_L + \Psi_N}{U_T}} - \left(1 - \cosh\left(\frac{PL}{2}\right) \right)} \right] \quad (42)$$

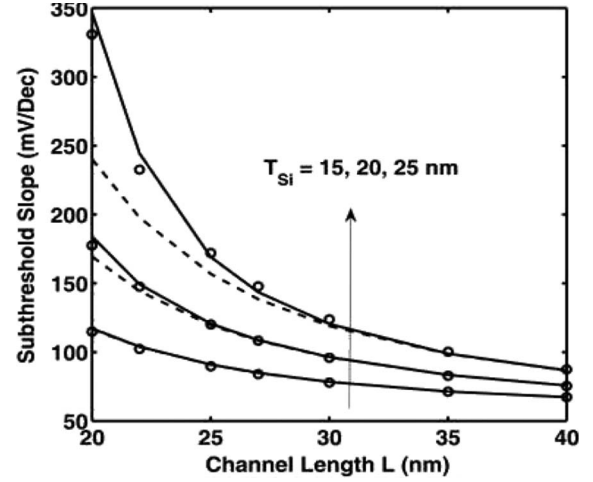


Fig. 6. Subthreshold slope variation with channel length L . Symbol represents data extracted from Atlas I_d-V_{gs} characteristics at low V_{ds} , and the solid line represents the model including $\Psi_N(x, y)$ component. The dotted line represents the subthreshold slope curve not considering $\Psi_N(x, y)$ component.

with

$$\alpha = \sum_{n=1}^{\infty} \left[\frac{\sinh\left(\frac{\mu_n L}{T_{Si}}\right) \cos\left(\frac{2\mu_n y}{T_{Si}}\right) \sin(\mu_n)}{\mu_n \sinh\left(\frac{2\mu_n L}{T_{Si}}\right) \left(\frac{2\epsilon_{Si} \sin^2(\mu_n)}{C_{ox} T_{Si}} + 1 \right)} \right]. \quad (43)$$

From Fig. 6, it is shown that the $\Psi_N(x, y)$ component plays a significant role in the subthreshold slope expression when the SCE is severe (devices having a higher T_{Si}/L ratio).

Finally, we would like to mention that a similar analysis of body potential has been carried out for the cylindrical Gate-All-Around (GAA) MOSFET [12], and it was found that for the GAA MOSFET, the effective conduction path is 33.3% away from the channel center whereas for the DG MOSFET it is 12.5% away. This is because the GAA MOSFET is more immune to the SCE than the DG MOSFET.

IV. CONCLUSION

In this paper, we present a novel technique for solving the 2-D nonlinear Poisson's equation analytically in a rectangular coordinate system. Using this technique, a new physically based classical potential distribution model for an undoped channel DG transistor is derived. The proposed model shows excellent accuracy with a professional device simulator in predicting the potential at any point of the body in both weak and strong inversion regimes. We demonstrated, using the proposed model, that the channel potential versus gate voltage characteristics for the devices having equal channel lengths but different body thicknesses pass through a single common "crossover point." A new compact model for the subthreshold slope is formulated from the proposed channel potential model. The improvement of the proposed model over the previous models is reflected in the low drain voltage subthreshold slope and SCE calculation.

APPENDIX

We solve the nonlinear PDE (19) in the neighborhood of the boundary $y = 0$ at which both the y dependent terms of the Laplace operator vanish ($(\partial\Psi_N/\partial y) \approx (\partial^2\Psi_N/\partial y^2) \approx 0$). Hence, the PDE reduces to an ordinary differential equation (ODE) of x where the terms dependent on y are treated as constants. Therefore, the resulting ODE takes the following form:

$$\frac{d^2\Psi_N}{dx^2} = \frac{q}{\epsilon_{Si}} n_i e^{\Psi_0/U_T} \left(e^{(\Psi_L + \Psi_N - \Psi_F)/U_T} - 1 \right). \quad (44)$$

Now, the variation of Ψ_F along the channel can be calculated only by solving the continuity equation consistently with Poisson's equation. However, from simulation, it is found that the variation of Ψ_F is very much similar to that of Ψ_L , and hence, we approximate Ψ_F with the following relation:

$$\Psi_L - \Psi_F \approx \Psi_{L0} \quad (45)$$

where Ψ_{L0} is the value of Ψ_L at $V_{ds} = 0$. Now, if we treat $\Psi_{L0}(x, y)$ also as a constant and substitute $z = (\Psi_{L0} + \Psi_N)/U_T$, then the aforementioned ODE (44) transforms into the following form:

$$\frac{d^2z}{dx^2} = P^2(e^z - 1) \quad (46)$$

$$\text{or } \frac{1}{2} \left(\frac{dz}{dx} \right)^2 = P^2(e^z - z) + C_0 \quad (47)$$

$$\text{or } \frac{1}{2} \left(\frac{dz}{dx} \right)^2 = z'' - P^2z + P^2 + C_0. \quad (48)$$

Now, we put $z' = 0$ in the LHS of (47) in order to calculate the value of the integration constant C_0 as $C_0 = P^2(z_{\min} - e^{z_{\min}})$. For a low V_{ds} , z_{\min} occurs near $x = L/2$. However, (48) cannot be solved analytically. Therefore, we approximate (48) by making the LHS zero, and this approximation works very well for the channel region away from S/D boundaries. Hence, the final ODE becomes

$$z'' - P^2z + P^2 + C_0 = 0 \quad (49)$$

which can be solved analytically and the final solution is given in (33).

ACKNOWLEDGMENT

The authors would like to thank Prof. R. Vittal Rao, Indian Institute of Science, for his valuable suggestions in solving PDEs.

REFERENCES

- [1] H. A. E. Hamid, J. R. Guitart, and B. Iniguez, "Two-dimensional analytical threshold voltage and subthreshold swing models of undoped symmetric double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 6, pp. 1402–1408, Jun. 2007.
- [2] X. Liang and Y. Taur, "A 2-D analytical solution for SCEs in DG MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1385–1391, Sep. 2004.

- [3] Q. Chen, E. M. Harrell, and J. D. Meindl, "A physical short-channel threshold voltage model for undoped symmetric double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 7, pp. 1631–1637, Jul. 2003.
- [4] S.-H. Oh, D. Monroe, and J. M. Hergenrother, "Analytic description of short-channel effects in fully-depleted double-gate and cylindrical, surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 445–447, Sep. 2000.
- [5] G. Pei, V. Narayanan, Z. Liu, and E. C. Kan, "3D analytical subthreshold and quantum mechanical analyses of double-gate MOSFET," in *IEDM Tech. Dig.*, 2001, pp. 5.3.1–5.3.4.
- [6] J. Song, B. Yu, C. Hsu, C. Cleavelin, M. Ma, P. Patruno, and Y. Taur, "Experimental hardware calibrated compact models for 50 nm n-channel FinFETs," in *Proc. SOI Conf.*, 2007, pp. 131–132.
- [7] B. Yu, H. Lu, M. Liu, and Y. Taur, "Explicit continuous models for double-gate and surrounding-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2715–2722, Oct. 2007.
- [8] J. Kou and Y. Li, "Modified Chebyshev–Halley methods with sixth-order convergence," *Appl. Math. Comput.*, vol. 188, no. 1, pp. 681–685, Jun. 2007.
- [9] *ATLAS User's Manual*, Silvaco Int., Santa Clara, CA, 2006, version 5.12.1.R.
- [10] B. El-Kareh, W. Tonti, and S. Titcomb, "A submicron MOSFET parameter extraction technique," *IBM J. Res. Develop.*, vol. 34, no. 2/3, pp. 243–249, Mar.–May 1990.
- [11] Q. Chen, B. Agrawal, and J. Meindl, "A comprehensive analytical subthreshold swing (S) model for double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 6, pp. 1086–1090, Jun. 2002.
- [12] B. Ray and S. Mahapatra, "Modeling and analysis of body potential of cylindrical gate-all-around nanowire transistor," *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2409–2416, Sep. 2008.



Biswajit Ray received the B.Tech degree in electrical and electronics engineering from National Institute of Technology, Trichy, India, in 2006 and the M.Sc. (Engg.) degree from Indian Institute of Science, Bangalore, India, in 2008. He is currently working toward the Ph.D. degree at the Purdue University, West Lafayette, IN.

His current research interests include compact modeling and simulation of semiconductor devices.



Santanu Mahapatra (M'08) received the B.E. degree in electronics and telecommunication from Jadavpur University, Kolkata, India, in 1999, the M.Tech. degree in electrical engineering with specialization in microelectronics from the Indian Institute of Technology, Kanpur, India, in 2001, and the Ph.D. degree in electrical engineering, from the Swiss Federal Institute of Technology Lausanne, Lausanne, Switzerland, in 2005, focusing on compact modeling of Single Electron Transistors and their hybridization with CMOS.

Since 2005, he has been an Assistant Professor with the Centre for Electronics Design and Technology (CEDT), Indian Institute of Science, Bangalore, India. He is the Founder of the Nano Scale Device Research Laboratory, CEDT, in 2006, where his team is engaged in research on compact modeling and simulation of emerging nanotechnologies and advanced CMOS devices. He provides consultancy to the device reliability group of Cypress Semiconductor, Bangalore. He is the author or coauthor of several papers published in international journals and refereed conferences. He is also the author of the book "Hybrid CMOS Single Electron Transistor Device and Circuit Design" (Artech House, 2006). His current research interests include device reliability, multigate transistors, tunnel field-effect transistors, single-electron transistors, and CMOS-nano hybridization.

Dr. Mahapatra received the Best Paper Award in the International Semiconductor Conference (CAS), Romania, in 2003. He is also the recipient of IBM Faculty Award in 2007 and Microsoft India Research Outstanding Faculty Award in 2007.