Nonquasi-Static Charge Model for Common Double-Gate MOSFETs Adapted to Gate Oxide Thickness Asymmetry

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***Abstract*— With the unique quasi-linear relationship between the surface potentials along the channel, recently we have proposed a quasi-static terminal charge model for common double-gate MOSFETs, which might have asymmetric gate oxide thickness. In this brief, we extend this concept to develop the nonquasi-static (NQS) charge model for the same by solving the governing continuity equations. The proposed NQS model shows good agreement against TCAD simulations and appears to be useful for efficient circuit simulation.**

***Index Terms*— Compact modeling, double-gate (DG) MOSFET, nonquasi-static (NQS) effect.**

I. Introduction

MULTIGATE MOSFETs have appeared as replacements for bulk MOSFETs in sub-32-nm technology nodes [1]–[3]. For successful utilization of these devices in RF circuit design, we need efficient compact models that include nonquasi-static (NQS) effects [4]. In professional compact models [5], [6], two different approaches, relaxation time approximation (RTA)- and continuity equation (CE)-based methods, are used for NQS modeling. Although RTA-based methodology is very simple to implement in a circuit simulator and promises faster convergence, it is less accurate at higher frequency domains and requires additional NQS measurement for the calibration of the model parameters associated with the relaxation time expression [7], [8]. On the other hand, NQS models, which are based on direct solution of the governing CE, are physics-based, valid for (in principle) any arbitrary range of operating frequency and do not involve any additional model parameters apart from those used in quasi-static (QS) model. CE-based models are, however, mathematically complicated than the RTA models and thus computationally expensive.

Though the multigate MOSFETs are expected to be realized by nonplanar technology where effect of the third gate may not be neglected, compact models for such devices are being developed by tweaking the planar double-gate (DG) MOSFET models [9], [10]. Existing compact models for planner common DG MOSFETs (CDG MOSFETs) [2], [11]–[13], i.e., both gates have the same work functions, which are based on the fundamental assumption that they have equal oxide thickness. For practical devices, it is most likely that the thicknesses of the two gate oxides are slightly different because of process variations and uncertainties, which can affect device performance significantly. With the unique quasi-linear relationship between the surface potentials along the channel, recently we have reported a QS charge model for a generic CDG MOSFET [14]. In this brief, we extend this concept to develop a CE approach-based NQS charge model for the same. Proposed model is shown to have good agreement with TCAD simulations [15] and appears to be useful for efficient circuit simulation.

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II. Model Development

The conventions used in this brief are as follows: $t_{\mathrm{ox1(2)}}$ is the oxide thickness of first (second) gate, t_{si} is the thickness of the silicon body, $C_{\mathrm{ox1(2)}}$ is the oxide capacitance per unit area of first (second) gate defined as $\epsilon_{\mathrm{ox}}/t_{\mathrm{ox1(2)}}$, ϵ_{si} and ϵ_{ox} are the permittivities of Si and SiO_2, respectively, q is the elementary charge, β is the inverse thermal voltage, n_i is the intrinsic carrier density, $B = 2qn_i/\beta\epsilon_{si}$, L is the channel length, W is the channel width, $\psi_{1(2)}$ are the Si/SiO_2 surface potentials at first (second) gate, V is the electron quasi-Fermi potential (channel potential), and μ is the effective mobility. The effective gate voltage with respect to source terminal is defined as $V_{\mathrm{gs}} = V_{\mathrm{gs,applied}} - \delta\phi$, where $V_{\mathrm{gs,applied}}$ is the voltage applied at gate terminals and $\delta\phi$ is the work-function difference of the gate material. V_{ds} is the applied drain voltage with respect to source terminal. The inversion charge density at any point along the channel is denoted by Q_i, which is the sum of two components Q_{i1} and Q_{i2} expressed as $Q_{i1(2)} = C_{\mathrm{ox1(2)}}(V_{\mathrm{gs}} - \psi_{1(2)})$. In the following discussion, any variable with subscript "s" refers to its values at source end and subscript "d" refers to its value at drain end.

It is demonstrated in [14] that in a QS situation, for any given bias condition, the surface potentials (i.e., ψ_1 and ψ_2) along the undoped channel hold a quasi-linear relationship. This is because both gates are connected together and they have the same work-function difference. The QS terminal charge model is developed by linearizing ψ_1 against ψ_2. In Fig. 1, through TCAD simulation, we show that such quasi-linear relationships also exist under NQS condition. Therefore,

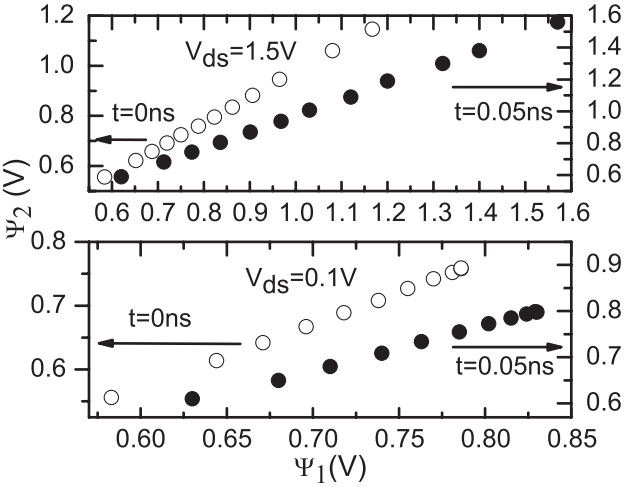

Fig. 1. Relationship between ψ_1 and ψ_2 in both linear and saturation regions. V_{gs} is swept from 1 to 1.5 V at ramp rate of 10 V/ns.

the same linearization technique can be used for developing the NQS charge model.

The governing CE for such devices can be expressed as follows:

$$\frac{\partial I}{\partial y} = -W\frac{\partial Q_i}{\partial t} \Rightarrow \frac{\partial}{\partial y}\left(\mu W Q_i \frac{dV}{dy}\right) = -W\frac{\partial Q_i}{\partial t} \quad (1)$$

where I is the drain current and V is the channel potential at any point y along the channel ($y = 0$ and L are the source and drain ends, respectively). Now, from the expression of the coupling factor G [14, eq. (4)], we arrive at the following:

$$V = V_{gs} - \frac{Q_{i1}}{C_{ox1}} - \frac{1}{\beta}\ln\left(\frac{1}{B}\left(nQ_{i1}^2 - G\right)\right) \quad (2)$$

where $n = 1/\epsilon_{si}^2$. Further applying linearization $G \simeq s_1 Q_{i1} + k_1$ [14] and differentiating (2) with respect to Q_{i1}, we obtain the following:

$$\frac{dV}{dQ_{i1}} = -\frac{1}{C_{ox1}} - \frac{1}{\beta}\frac{(2nQ_{i1} + s_1)}{\left(nQ_{i1}^2 + s_1 Q_{i1} + k_1\right)} \quad (3)$$

with $s_1 = -(G_d - G_s)/(Q_{i1d} - Q_{i1s})$ and $k_1 = -(G_s Q_{i1d} - G_d Q_{i1s})/(Q_{i1d} - Q_{i1s})$. Again linearizing Q_{i2} with respect to Q_{i1} as $Q_{i2} \simeq m_1 Q_{i1} + c_1$, we get the following:

$$Q_i = Q_{i1} + m_1 Q_{i1} + c_1 \quad (4)$$

with $m_1 = (Q_{i2s} - Q_{i2d})/(Q_{i1s} - Q_{i1d})$ and $c_1 = (Q_{i1s}Q_{i2d} - Q_{i2s}Q_{i1d})/(Q_{i1s} - Q_{i1d})$. Using (4) and (3) in (1) and introducing normalized variables: $y' = y/L$, $t' = t/(L^2/\mu)$, we obtain the modified form of the CE as follows:

$$\frac{\partial Q_i}{\partial t'} = \frac{\partial^2 Q_i}{\partial y'^2} f(Q_i) + u(Q_i)\left(\frac{\partial Q_i}{\partial y'}\right)^2 \quad (5)$$

where

$$f(Q_i) = \frac{Q_i}{C_{ox1}(m_1+1)} + \frac{Q_i\left(2n(Q_i - c_1) + s_1(m_1+1)\right)}{\beta\Upsilon} \quad (6)$$

$$u(Q_i) = \frac{1}{C_{ox1}(m_1+1)} + \frac{\Xi}{\beta} + \frac{2nQ_i}{\beta\Upsilon} + \frac{\Xi Q_i}{\beta} \quad (7)$$

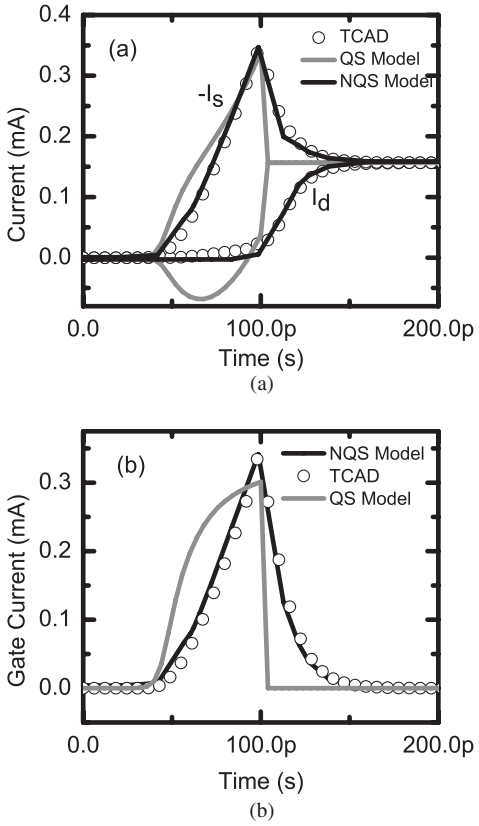

Fig. 2. (a) Drain (I_d) and source (I_s). (b) Gate terminal currents predicted by proposed model and the TCAD simulation. A step voltage from 0 to 1 V is applied to gate with a rise time of 100 ps and V_{ds} is kept at 1 V.

with $\Upsilon = (n(Q_i - c_1)^2 + s_1(1+m_1)(Q_i - c_1) + k_1(1+m_1)^2)$ and $\Xi = (2n(Q_i - c_1) + s_1(1+m_1))/\Upsilon$. To obtain the Q_i distribution over y at time t, we need to solve (5) with the boundary condition $Q_i(y = 0, t) = Q_{is}$ and $Q_i(y = L, t) = Q_{id}$ and using the initial condition $Q_i(y, 0)$, which could be obtained by inverting the y versus Q_{i1} relationship [14, eq. (4)]. We assume Q_{is} and Q_{id} change instantaneously with terminal voltages (i.e., no NQS effect) [8], [11], hence they can be calculated by solving the input voltage equations (IVEs) [16] for the bias conditions at time t. Though this assumption does not hold good at drain end in weak or moderate inversion, it is reasonable as the QS Q_{id} itself is very small under these conditions. Once we obtain $Q_i(y, t)$, the terminal charges could be computed by solving the terminal charge integrals [14, eq. (18)–(20)]. To solve such partial differential equation (PDE) inside a circuit simulator, however, one needs to convert it in a set of ordinary differential equations (ODEs). Several techniques were available in literature [17]–[19] to convert PDE into ODEs. In this brief, we have used spline collocation method as it is already implemented in professional circuit simulator [8]. In a four-point spline collocation method, if the inversion charges are defined as $q_0 = Q_i(y' = 0) = Q_{is}$, $q_1 = Q_i(y' = 1/5)$, $q_2 = Q_i(y' = 2/5)$, $q_3 = Q_i(y' = 3/5)$, $q_4 = Q_i(y' = 4/5)$, and $q_5 = q(y' = 1) = Q_{id}$, (5) could be converted into following four coupled ODEs [11], [21] as follows:

$$\frac{dq_j}{dt'} = a_j f(q_j) + u(q_j)\left(b_j\right)^2 \quad (8)$$

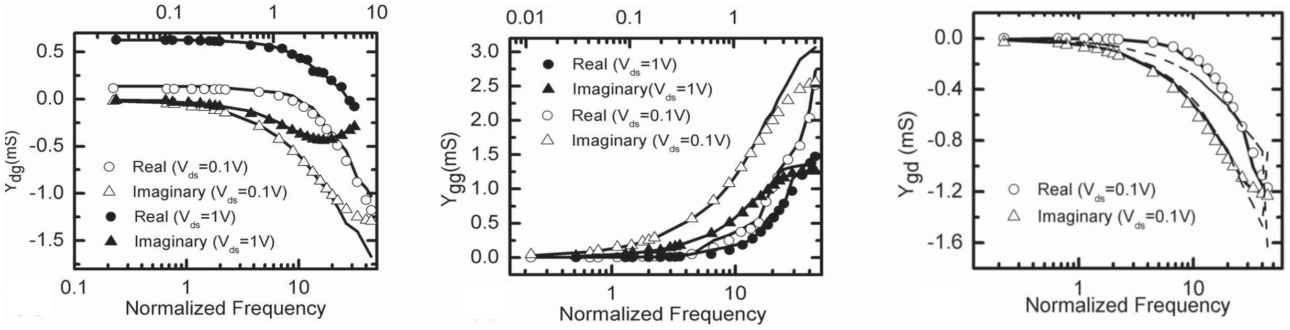

Fig. 3. Small signal characteristics: (a) Y_{dg}, (b) $Y_{\rm gg}$, and (c) $Y_{\rm gd}$ as predicted by the TCAD (symbol) and the proposed model (line). In all plots, $V_{\rm gs}$ is kept at 1 V. In (c), the dashed line represents proposed model with two-point collocation technique. Y at $V_{\rm ds} = 1$ V is plotted against top x-axis that is normalized to 3.3 GHz and Y at $V_{\rm ds} = 0.1$ V is plotted against bottom x-axis that is normalized to 0.45 GHz.

where j varies from 1 to 4 and

$$a_1 = \frac{1350q_2 - 1905q_1 - 360q_3 + 90q_4 - 15q_5 + 840q_0}{209/10} \quad (9)$$

$$a_2 = \frac{1350q_1 - 2265q_2 + 1440q_3 - 360q_4 + 60q_5 - 225q_0}{209/10} \quad (10)$$

$$a_3 = \frac{1440q_2 - 360q_1 - 2265q_3 + 1350q_4 - 225q_5 + 60q_0}{209/10} \quad (11)$$

$$a_4 = \frac{90q_1 - 360q_2 + 1350q_3 - 1905q_4 + 840q_5 - 15q_0}{209/10} \quad (12)$$

$$b_1 = \frac{900q_2 - 225q_1 - 240q_3 + 60q_4 - 10q_5 - 485q_0}{209} \quad (13)$$

$$b_2 = \frac{840q_3 - 15q_2 - 780q_1 - 210q_4 + 35q_5 + 130q_0}{209} \quad (14)$$

$$b_3 = \frac{210q_1 - 840q_2 + 15q_3 + 780q_4 - 130q_5 - 35q_0}{209} \quad (15)$$

$$b_4 = \frac{240q_2 - 900q_3 - 60q_1 + 225q_4 + 485q_5 + 10q_0}{209}. \quad (16)$$

These four ODEs could be solved inside a circuit simulator in a subcircuit approach [8]. Similar to QS model [14], the proposed NQS model is also derivative free, i.e., the derivative of the IVE does not enter in the expression of the large signal model.

III. Results and Discussions

We have validated our model against the 2-D TCAD simulation results [15] for devices having gate oxide thickness asymmetry: $t_{\rm ox1} = 1$ nm, $t_{\rm ox2} = 2$ nm, $t_{si} = 10$ nm, $L = 1$ μm, and $W = 1$ μm. The cutoff frequency (f_t) is calculated as $f_t = g_m/(2\pi C_{\rm gg})$ and are found to be $\sim$3.3 GHz at $V_{\rm gs} = V_{\rm ds} = 1$ V and $\sim$0.45 GHz at $V_{\rm gs} = 1$; $V_{\rm ds} = 0.1$ V (here g_m is the gate transconductance and $C_{\rm gg}$ is gate–gate capacitance). The channel is kept undoped and source–drain doping is taken as 10^{20} cm^{-3}. We use constant mobility of 300 cm^2/V-s both in TCAD simulation and proposed model. We have solved (8) in MATLAB [20] to obtain q_j, which is then used to calculate the NQS terminal charges [11], [21].

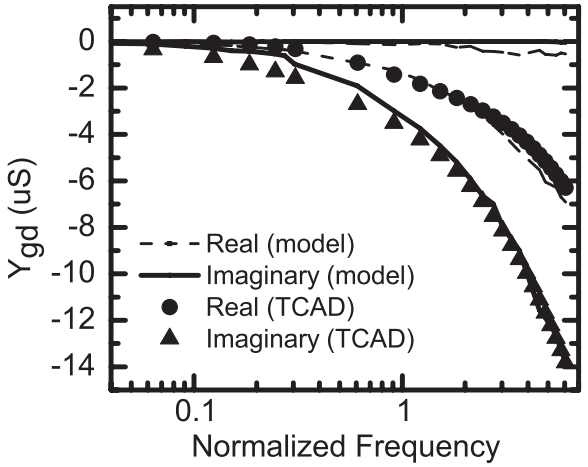

Fig. 4. $Y_{\rm gd}$ predicted by proposed model with and without incorporation of channel-length modulation (CLM) and the TCAD simulation. $V_{\rm gs} = V_{\rm ds}$ is kept at 1 V. Frequency is normalized to 3.3 GHz.

Fig. 2 shows the transient behavior of terminal currents while the gate voltage changes from 0 to 1 V in 100 ps. This rise time is chosen to ensure NQS condition as the transit time ($1/f_t$) of the carriers found to be 300 ps. We can see that the proposed model predicts the transient behavior of the terminal currents with superior accuracy in comparison with the QS model. The variation for the real and imaginary components of different small signal Y parameters as a function of frequency is shown in Fig. 4(a)–(c) under both saturation and linear bias conditions. With a four-point collocation technique, the proposed model predicts the Y parameters quite accurately up to a frequency range of $5f_t$ for saturation bias condition and $30f_t$ for linear bias condition, which is more than double what could be achieved in a RTA-based method [7]. As shown in Fig. 4(c), a two-point collocation technique, however, shows a significant mismatch even at f_t. The $Y_{\rm gd}$ characteristics at saturation is shown in Fig. 4 and mismatch is observed between the model and the TCAD data. Proposed model predicts $Y_{\rm gd}$ to be zero in saturation as it is based on gradual channel approximation while CLM is not considered. Some amount of CLM is, however, observed in the TCAD simulation even for a channel length of 1 μm. Though this CLM is very small, it shows significant effect in $Y_{\rm gd}$ characteristics

in saturation as change of the terminal charges because of drain voltage variation itself is extremely small. If we use a basic CLM model by introducing effective channel length as $L_{\text{eff}} = L \times (1 - \lambda V_{\text{ds}})$, we can match the TCAD result with proper tuning of λ. Y_{gd} in saturation is 100 times lower than its linear value and hence is not very significant in circuit designing.

Finally, complexity of the proposed model is the same as that of the symmetric devices [11]. The proposed model, however, inherits computational overhead of solving the complex IVEs of asymmetric devices [16]. Moreover, in small oxide thickness asymmetry (which is expected in practical devices), the surface potentials could be computed by a simple perturbation technique [14] without sacrificing any significant computation time.

IV. Conclusion

With the quasi-linear relationship between the surface potentials, we proposed a new NQS charge model for CDG MOSFETs, which might have differences in gate oxide thickness. Proposed models were verified against TCAD simulation and appeared to be promising for efficient circuit simulation.

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