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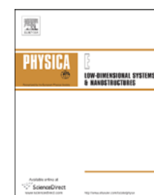

Modeling and analysis of energy quantization effects on single electron inverter performance ☆

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ABSTRACT

In this paper, for the first time, the effects of energy quantization on single electron transistor (SET) inverter performance are analyzed through analytical modeling and Monte Carlo simulations. It is shown that energy quantization mainly changes the Coulomb blockade region and drain current of SET devices and thus affects the noise margin, power dissipation, and the propagation delay of SET inverter. A new analytical model for the noise margin of SET inverter is proposed which includes the energy quantization effects. Using the noise margin as a metric, the robustness of SET inverter is studied against the effects of energy quantization. A compact expression is developed for a novel parameter *quantization threshold* which is introduced for the first time in this paper. Quantization threshold explicitly defines the maximum energy quantization that an SET inverter logic circuit can withstand before its noise margin falls below a specified tolerance level. It is found that SET inverter designed with $C_T : C_G = 1/3$ (where C_T and C_G are tunnel junction and gate capacitances, respectively) offers maximum robustness against energy quantization.

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1. Introduction

In recent past, the hybridization of single electron transistor (SET) with complementary metal oxide semiconductor (CMOS) technology has attracted much attention [1–3]. Such integration can offer new functionalities, which are very difficult to achieve either by pure CMOS or by pure SET approaches. As a result, silicon SETs are appearing to be more promising than metallic SETs for their possible integration with CMOS. SETs are normally studied on the basis of the classical orthodox theory [10], where quantization of energy states in the island is completely ignored. Though this assumption greatly simplifies the physics involved, it is valid only when the SET is made of metallic island. As one cannot neglect the energy quantization in a semiconductive island, it is extremely important to study the effects of energy quantization on silicon SET logic performance.

In this paper, for the first time, the effects of energy quantization on voltage-state SET inverter performance are analyzed using Monte Carlo (MC) simulations. It is found that energy quantization primarily alters the Coulomb blockade region and the drain current of SET devices and thereby it affects the noise margin, power dissipation, and the propagation delay of the SET inverter. A simple analytical model is proposed for the noise margin of SET inverter by including the energy quantization effect, which would be very useful for circuit designer. Using the noise margin as a metric, the robustness of SET inverter is studied against energy quantization. It is found that SET inverter designed with $C_T : C_G = 1/3$ (where C_T and C_G are tunnel junction and gate capacitances, respectively) offers maximum robustness against the energy quantization.

2. The Monte Carlo simulation

2.1. Simulation of discrete energy states using SIMON

The total tunnel rate from the occupied states (initial states i) on one side of the barrier to the unoccupied states (final states f) of the other side of the barrier, considering the change in free energy and using Fermi's Golden Rule can be expressed as the following summation [4]:

$$\Gamma(\Delta G) = \frac{2\pi}{\hbar}\sum_i \sum_f |T_{if}|^2 f(E_i)\{1 - f(E_f)\} \times \delta(E_i - E_f - \Delta G) \tag{1}$$

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where T_{if} is the tunnel transmission coefficient and $f(E)$ is the Fermi-Dirac distribution. Using the density of states $D(E)$, the above summation can be changed into the following integrals over energy:

$$\Gamma(\Delta G) = \frac{2\pi}{\hbar}|T_{if}|^2 \int_{E_{c,i}}^{\infty}\int_{E_{c,f}}^{\infty} D_i(E_i)D_f(E_f)f(E_i) \times\{1-f(E_f)\}\delta(E_i - E_f - \Delta G)\,dE_f\,dE_i \quad (2)$$

where $E_{c,i}$ ($E_{c,f}$) is the conduction band edge of the side where electron resides initially, initial side (tunneling to, final side), and $D_i(E_i)$ and $D_f(E_f)$ are the density of states or DOS on the initial and final side of the barrier. For metallic islands, the DOS D_i and D_f may be considered as constant in the small window of energy $f(E_i)\{1-f(E_f)\}$ and can be taken out of the integral reducing Eq. (2) to

$$\Gamma(\Delta G) = \frac{2\pi}{\hbar}|T_{if}|^2 D_i D_f \int_{\max(E_{c,i},E_{c,f})}^{\infty} f(E)\{1-f(E)\}\,dE \quad (3)$$

Evaluating this integral gives us the orthodox theory expression for single electron tunneling rate given by

$$\Gamma(\Delta G) = \frac{\Delta G}{e^2 R_T\{1-\exp(-\Delta G/k_B T)\}} \quad (4)$$

where ΔG denotes the change in Gibb's free energy of the electron during tunneling, e, k_B and T denote the elementary charge, Boltzmann constant and the temperature (in Kelvin), respectively, and $R_T = \hbar/2\pi e^2\hbar|T_{if}|^2 D_i D_f$ denotes the phenomenological quantity called '*tunneling resistance*'. In SIMON R_T has to be specified by the user.

For non-metallic islands with discrete energy levels, in order to calculate the total tunneling rate one typically starts from Fermi's Golden Rule as above. The only difference is that now we cannot take $D_f(E_f)$ as a constant since the DOS for a discrete energy spectrum is a sum of delta-functions. A more realistic treatment would be to consider finite life-time broadening which introduces the Lorentzian shape functions instead of the delta functions given by [5]

$$D_f(E_f) = \frac{\hbar}{2\pi}\sum_n \frac{\gamma}{(E_n - E)^2 + (\hbar\gamma/2)^2} \quad (5)$$

where E_n are the discrete energy levels (due to quantization) in the island, which determines the position of the energy levels while γ denotes the *total exit rate* from any particular energy state, which determines the shape of the Lorentzian function. For $\gamma \to 0$, the Lorentzian approaches an ideal delta function. Using this formulation, deriving the tunneling rate expression from first principles (as followed in orthodox theory) for the realistic case of infinite number of energy states, leads to the same expression (Eq. (4)), with the tunneling resistance term changing into

$$R'_T = R_T \Bigg/ \left[\frac{(\gamma/D_f)}{(E_n - E)^2 + (\hbar\gamma/2)^2}\right] \quad (6)$$

The height $H = (\gamma/D_f)$ and width $W = (\hbar\gamma/2)$ parameters in SIMON which define the Lorentzian shape, are constants related to the total exit rate from any particular energy state (γ) [4–7] and need to be tuned manually as discussed in the following section.

Simulating energy quantization effect in SIMON is not so straight forward like simulating metallic SETs where energy quantization was ignored. To our best knowledge, in this work, for the first time, we demonstrate how to use SIMON simulator in order to analyze energy quantization effect on SET device and circuit performance. It is worth noting that in this work, we have not attempted to deal with the complex quantum physics involved in obtaining a definite value of the energy gap between two successive energy levels (ΔE) for any particular device geometry. Here ΔE is treated as an *electrical parameter* so that we can study 'what happens when' the energy quantization is gradually introduced in a metallic SET without detailing how to obtain the exact value of ΔE for the structure. The problem of developing analytical expressions for the quantum physics involved in ΔE, itself is a complicated work and *not* the objective of this paper.

2.2. Tuning the simulator for capturing the quantization effects

The schematic of an SET device is shown in Fig. 1. One may conceptualize a metallic SET to be equivalent to a non-metallic one in which the energy states of the island extend from lower bound $E_{min} \to -\infty$ to upper bound $E_{max} \to +\infty$ with the energy gaps between successive energy states $\Delta E \to 0$. In order to study the energy quantization effects, we first simulate an SET with metallic (continuous energy spectrum) island for a particular set of device parameters (C_G, C_T~aF and R_T~$M\Omega$). Then, for the same set of device parameters, we simulate a non-metallic SET with discrete states, where $E_{min} = -1$ eV, $E_{max} = 1$ eV and $\Delta E = 0.001$ meV. As E_{min} and E_{max} values are much larger and ΔE is much smaller than the charging energy (~40 meV) of the SET, we can expect that such a device should behave as a metallic SET if the W and H parameters are properly tuned. By '*tuning*' we mean that to find proper values of H and W so that for a given set of device parameters (C_G, C_T, and R_T), when the energy gaps (ΔE) between adjacent energy levels are extremely smaller than the charging energy (e^2/C_Σ, where $C_\Sigma = C_G + 2C_T$ denotes the net capacitance seen by the island with respect to ground) and the number of energy levels are (practically) infinite, then the factor $[(\gamma/D_f)/\{(E_n - E)^2 + (\hbar\gamma/2)^2\}]$ in Eq. (6) tends to unity, i.e. $R'_T \to R_T$. After exhaustive simulations we have found that for $H = 0.04$ and $W = 0.001$, the $I-V$ characteristics of the non-metallic SET with discrete energy states completely super-imposes over the characteristics obtained from the metallic SET. It is further observed that these values of H and W are completely independent of device capacitances and resistances as long as their values lie in the range of aF and $M\Omega$, respectively. Using these tuned values of H and W, keeping E_{max} and E_{min} constant, we increase the value of ΔE in order to simulate the effects of energy quantization on SET device and inverter performances.

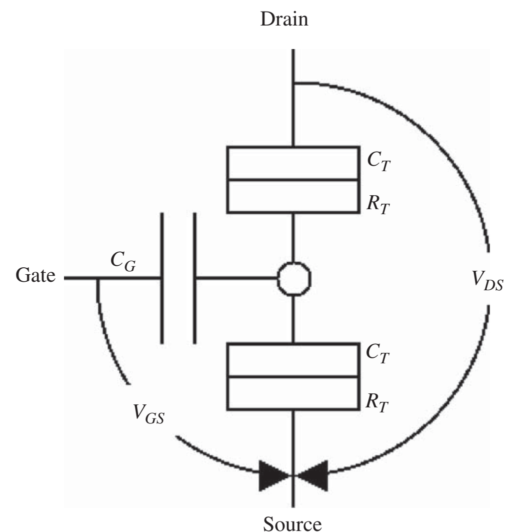


Fig. 1. Schematic diagram of a single electron transistor showing the different device parameters, C_G is the gate capacitance, while C_T and R_T are the capacitance and resistance of the tunnel barrier, respectively.

3. Results and discussions

In this paper, quantization effects are studied by gradually increasing the energy gaps ΔE between successive energy levels in the island of an SET as described in Section 2.2. When energy quantization is introduced, the net change in electron energy of the electrons during tunneling becomes the sum of electrostatic energy contributed by Coulomb blockade as well as the energy gaps between the quantized energy levels. Consequently, including the quantization term ΔE into the expression for the net energy change ΔF (which includes both Gibb's free energy ΔG and excitation/quantization energy ΔE) we obtain [8–11]

$$\Delta F_{s,i} = \frac{e}{C_\Sigma}\left[C_T V_{DS} + C_G V_{GS} - ne - \frac{e}{2}\right] - (n+1)\Delta E \tag{7}$$

$$\Delta F_{i,s} = \frac{e}{C_\Sigma}\left[-C_T V_{DS} - C_G V_{GS} + ne - \frac{e}{2}\right] - (n+1)\Delta E \tag{8}$$

$$\Delta F_{i,d} = \frac{e}{C_\Sigma}\left[(C_T + C_G) V_{DS} - C_G V_{GS} + ne - \frac{e}{2}\right] - (n+1)\Delta E \tag{9}$$

$$\Delta F_{d,i} = \frac{e}{C_\Sigma}\left[-(C_T + C_G) V_{DS} + C_G V_{GS} - ne - \frac{e}{2}\right] - (n+1)\Delta E \tag{10}$$

Here n denotes the number of discrete energy states in the island occupied by electrons and $\Delta F_{initial,final}$ denotes the net energy change for electron tunneling from the '*initial*' to the '*final*' regions, where '*initial*' and '*final*' regions can be any of the source, island or the drain terminals, respectively.

Conceptually one might approach the energy quantization problem in two ways: one is the way SIMON handles it, by replacing D_f in the orthodox model with its discrete equivalent, given in Eq. (5), and keeping the net energy change term (ΔF) in Eqs. (7)–(10) equal to the Gibb's free energy change ΔG, excluding the energy quantization term involving ΔE. The other approach, which is more elegant for developing the compact model is to consider energy quantization as an additive term to the Gibb's free energy resulting in the expressions for *net* energy change ΔF as given in Eqs. (7)–(10), and keeping the D_f term constant as in orthodox theory. This approach is accurate when the energy gaps between successive energy levels inside the island is extremely small compared to the electron charging energy e^2/C_Σ and there are (practically) infinite number of energy levels in the island. This situation is quite realistic in case of semiconductor islands where the quantized energy gaps between the adjacent energy levels are few orders of magnitude lower than the charging energy at practically realizable SET dimensions. The later approach we use in this work to develop noise margin model for SET inverter and it gives good agreement SIMON simulation.

3.1. Analysis of the energy quantization effects on SET device performance

Fig. 2 shows the influence of energy quantization on the $I_D - V_{GS}$ characteristics of the SET. It is evident from Fig. 2a that increasing energy quantization reduces the drain current I_D, as if the effective tunnel resistance R_T has increased. This could be understood from Eqs. (7)–(10), where the net energy change ΔF decreases linearly with increasing energy quantization ΔE, which in turn decreases the drain current I_D. Fig. 2b shows the influence of energy quantization and temperature on $I_D - V_{GS}$ plotted on a semilog scale. It is distinct from Fig. 2 that the entire $I_D - V_{GS}$ characteristics begin to shift towards the right with increasing ΔE, thus, in effect, the Coulomb blockade region increases. This can be theoretically explained as follows. In Eqs. (7)–(10), considering spin degeneracy of the electrons, there can be only one electron in each discrete energy state, implying that the number of occupied

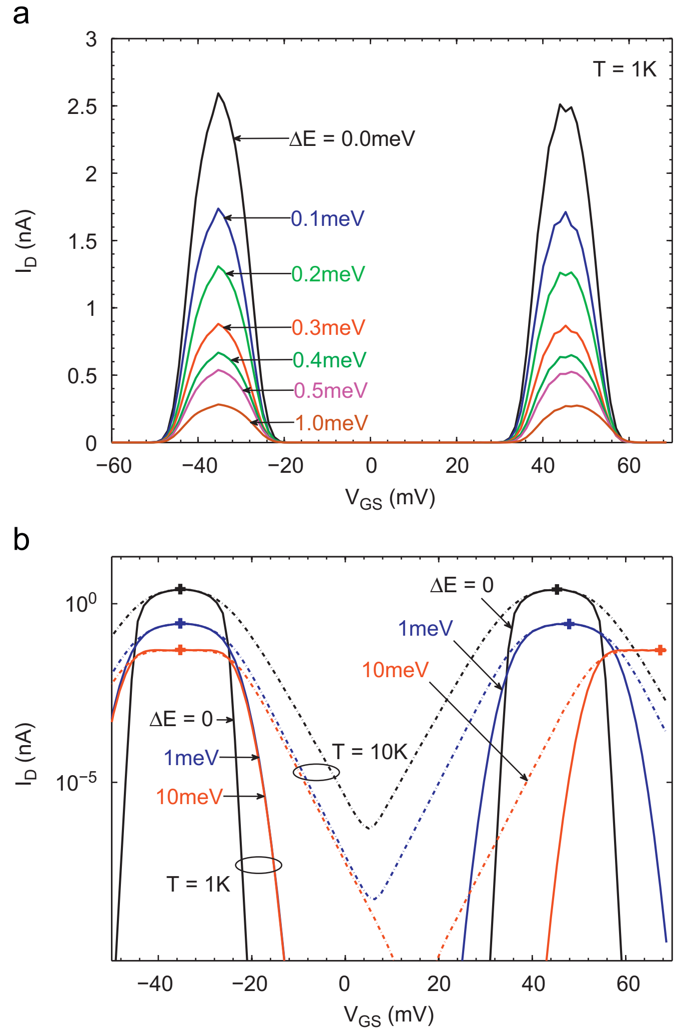


Fig. 2. Influence of energy quantization ΔE on $I_D - V_{GS}$ characteristics of an SET plotted on (a) linear and (b) logarithmic scale (simulated for $V_{DS} = 10$ mV, tunnel resistance $R_T = 1$ MΩ, gate capacitance $C_G = 2$ aF, tunnel capacitance $C_T = 1$ aF and in (a) $T = 1$ K).

energy states in the island (n) becomes equal to the number of electrons in the island. Then, expanding and rearranging Eqs. (7)–(10), it is found that the Coulomb blockade periodicity is increased from $(e/2C_G)$ to $(e/2C_G + \Delta E/e)$. Fig. 2b also shows the influence of temperature T on device behavior. It is found that increase of temperature reduces the Coulomb blockade region. Fig. 3 shows the influence of energy quantization on the $I_D - V_{DS}$ characteristics of the SET device, which also shows the decrease of drain current with increasing energy quantization. The increase in Coulomb blockade region in SETs due to energy quantization might be advantageous for applying higher drain voltage (i.e. more than e/C_Σ) and higher temperature operation.

3.2. Analysis of the energy quantization effects on SET inverter performance

Fig. 4 shows the schematic of the voltage-state SET inverter used in this work, where both the transistors T_1 and T_2 are completely identical in terms of device capacitances and resistances. Fig. 5 shows the influence of energy quantization on SET inverter transfer (V_{OUT} vs. V_{IN}) characteristics. These figures indicate that increasing energy quantization ΔE shifts the inverter

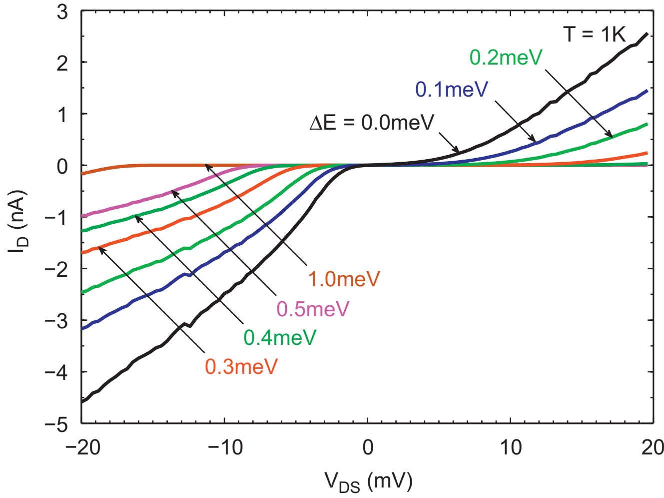


Fig. 3. Influence of energy quantization ΔE on $I_D - V_{DS}$ characteristics of an SET (simulated for $V_{GS} = 1\,\mathrm{V}$, $R_T = 1\,\mathrm{M\Omega}$, $C_G = 2\,\mathrm{aF}$, $C_T = 1\,\mathrm{aF}$, and $T = 1\,\mathrm{K}$).

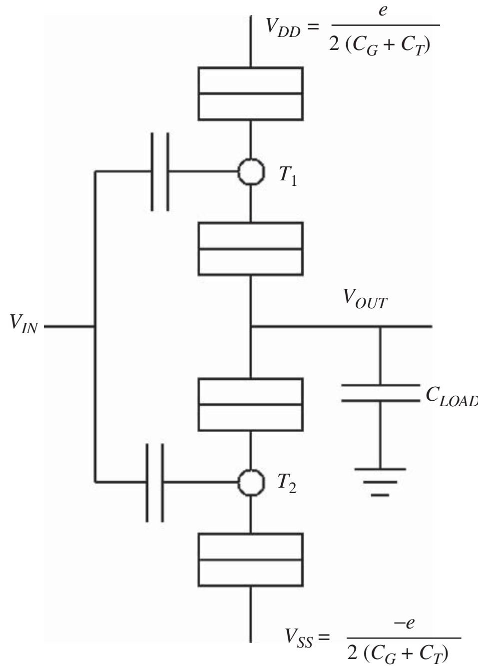
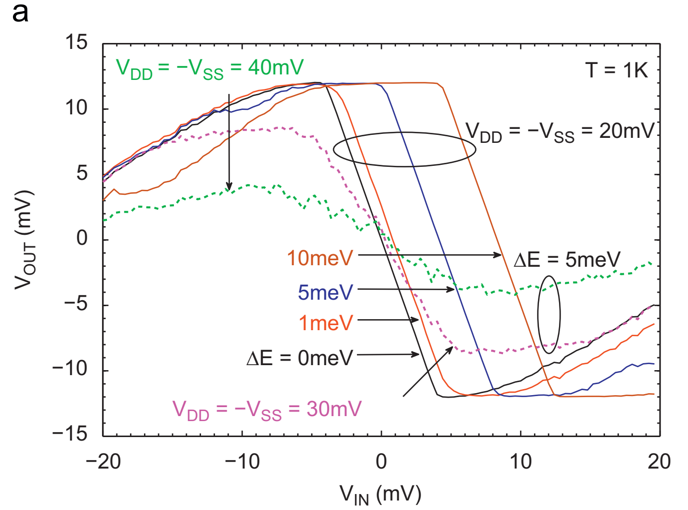


Fig. 4. Schematic diagram of a voltage-state SET inverter (SETs T_1 and T_2 are identical with load capacitance C_{LOAD}~fF).

V_{OUT} vs. V_{IN} characteristics towards the right, implying that larger input voltage V_{IN} is required for switching of a non-metallic SET with quantized energy states than its metallic counterpart. This is analogous to the influence of *fixed* positive background charges in the island, as described in Ref. [12]. It might be possible to compensate this horizontal shift by adding a second gate to SET island with appropriate control bias. It can also be seen from Fig. 5a and b that the inverter gain in logic transition region increases with decreasing $C_T : C_G$ ratio. Fig. 5 also demonstrate the fact that increasing supply voltage degrades the inverter performance. Therefore the supply voltage values $V_{DD} = -V_{SS} = e/2(C_G + C_T)$ which are optimum [3] for metallic-SET inverter also appear to be optimum in presence of energy quantization. Fig. 6 shows the influence of energy quantization and temperature on the static power dissipated by the SET inverter. Here P_{STATIC} is



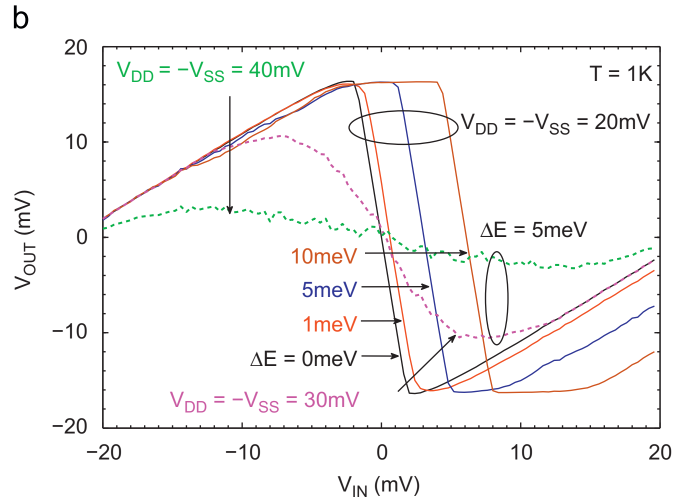


Fig. 5. Influence of energy quantization ΔE and bias $V_{DD}(= -V_{SS})$ on V_{OUT} vs. V_{IN} characteristics for different $\alpha = C_T/C_G$ ratios. Bold lines represent transfer characteristics for different ΔE at constant $V_{DD} = -V_{SS} = 20\,\mathrm{mV}$ while the broken lines represent transfer characteristics for different $V_{DD} = -V_{SS}$ at constant $\Delta E = 5\,\mathrm{meV}$, plotted for capacitance ratio (a) $\alpha = C_T/C_G = 1/3$ and (b) $\alpha = C_T/C_G = 1/9$ (simulated for $R_T = 1\,\mathrm{M\Omega}$, $C_G + C_T = 4\,\mathrm{aF}$, and $C_{LOAD} = 1\,\mathrm{fF}$).

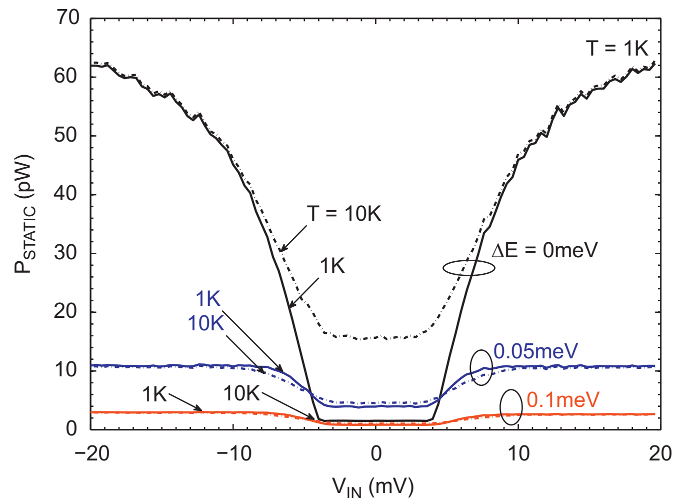


Fig. 6. Influence of energy quantization ΔE on power dissipation characteristics of an SET inverter (simulated for $V_{DD} = -V_{SS} = 20\,\mathrm{mV}$, $R_T = 1\,\mathrm{M\Omega}$, $C_G = 3\,\mathrm{aF}$, $C_T = 1\,\mathrm{aF}$, and $C_{LOAD} = 1\,\mathrm{fF}$).

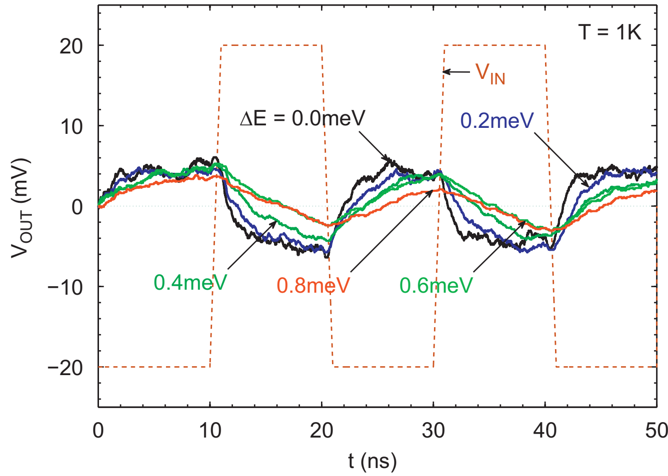


Fig. 7. Influence of energy quantization ΔE on delay characteristics of the SET inverter (simulated for $V_{DD} = -V_{SS} = 20\,\mathrm{mV}$, $R_T = 1\,\mathrm{M\Omega}$, $C_G = 3\,\mathrm{aF}$, $C_T = 1\,\mathrm{aF}$, and $C_{LOAD} = 1\,\mathrm{fF}$).

calculated as $P_{STATIC} = (V_{DD} - V_{SS})I_{STATIC}$ where I_{STATIC} is the steady state current flowing from V_{DD} to V_{SS} [3,12]. It can be inferred Fig. 6 that there is an enormous reduction in the power dissipation due to the degradation of I_D with increasing energy quantization.Fig. 6 also shows that power dissipation increases with increasing temperature because of the increase of leakage current in Coulomb blockade region as shown in Fig. 2b. Fig. 7 shows the variations of V_{OUT} with time t indicating the effect of energy quantization on the propagation delay of the SET inverter. It can be seen that the delay characteristics simply deteriorates as the drive current decreases with increasing ΔE.

4. Modeling of inverter noise margin with energy quantization

4.1. Development of the analytical model

The expressions for orthodox noise margin (NM) parameters were derived in Ref. [12] as

$$V_{OH} = -V_{OL} = \frac{\alpha V_{DD}}{2\alpha^2 + \alpha + 1} \tag{11}$$

$$V_{IH} = -V_{IL} = \frac{\alpha^2 V_{DD}}{2\alpha^2 + \alpha + 1} \tag{12}$$

$$NM = NM_H = NM_L = \frac{\alpha(1-\alpha)V_{DD}}{2\alpha^2 + \alpha + 1} \tag{13}$$

Inclusion of energy quantization alters the above noise margin parameters into the following expressions (refer to the Appendix):

$$V'_{OH} = V_{OH} - \left(\frac{1}{2\alpha^2 + \alpha + 1}\right)\frac{\Delta E}{e} \tag{14}$$

$$V'_{OL} = V_{OL} - \left(\frac{1}{2\alpha^2 + \alpha + 1}\right)\frac{\Delta E}{e} \tag{15}$$

$$V'_{IH} = V_{IH} + \left(\frac{2\alpha^2 + 2\alpha + 1}{2\alpha^2 + \alpha + 1}\right)\frac{\Delta E}{e} \tag{16}$$

$$V'_{IL} = V_{IL} + \left(\frac{2\alpha^2 + 2\alpha + 1}{2\alpha^2 + \alpha + 1}\right)\frac{\Delta E}{e} \tag{17}$$

Throughout this paper, *primed variables* (′) refer to the quantities including energy quantization effects, while unprimed variables refer to the ideal classical situation with the metallic SETs, following the orthodox theory of single electron tunneling. Eqs. (16) and (17) indicate that the entire transfer characteristics shift towards the right by the amount $\Delta E(2\alpha^2 + 2\alpha + 1)/(2\alpha^2 + \alpha + 1)e$ with respect to the orthodox characteristics. Eqs. (14) and (15) show that both the output voltage levels decrease simultaneously by $\Delta E/(2\alpha^2 + \alpha + 1)e$.

From the basic definitions of noise margins $NM_H \triangleq V_{OH} - V_{IH}$ and $NM_L \triangleq V_{IL} - V_{OL}$ we obtain (refer to the Appendix)

$$NM'_H = NM - 2\left(\frac{\alpha^2 + \alpha + 1}{2\alpha^2 + \alpha + 1}\right)\frac{\Delta E}{e} \tag{18}$$

$$NM'_L = NM + 2\left(\frac{\alpha^2 + \alpha + 1}{2\alpha^2 + \alpha + 1}\right)\frac{\Delta E}{e} \tag{19}$$

From Eqs. (18)–(19) it is evident that energy quantization increases the noise margin for low logic and decreases the noise margin for high logic by the same amount $2\Delta E(\alpha^2 + \alpha + 1)/(2\alpha^2 + \alpha + 1)e$. Thus it is seen that for the continuous spectrum ($\Delta E = 0$), Eqs. (18)–(19) reduces to orthodox model of noise margin as proposed in our earlier work [12]. It is worth noting that in Eqs. (18)–(19), the change in noise margins due to energy quantization, i.e. $2\Delta E(\alpha^2 + \alpha + 1)/(2\alpha^2 + \alpha + 1)e$, vary intensely with α, which explains the sharper switching in Fig. 5b than in Fig. 5a.

4.2. Validation of the model with simulation results

From the inverter transfer characteristics simulated in SIMON for different α and ΔE, the values of V_{OH}, V_{OL}, V_{IH}, and V_{IL} are recorded and the corresponding NM_H and NM_L are calculated. These values are plotted in Fig. 8, and it shows the variation of normalized noise margins with energy quantization. Fig. 8 also demonstrates the excellent agreement between the proposed model equation (18) and (19) and the simulated results.

4.3. Robustness of SET logic inverter against energy quantization and quantization threshold

Here we introduce a novel parameter *quantization threshold* (ΔE_{TH}) which may be defined as the maximum allowable energy quantization, for a given capacitance ratio $\alpha = C_T/C_G$, which the

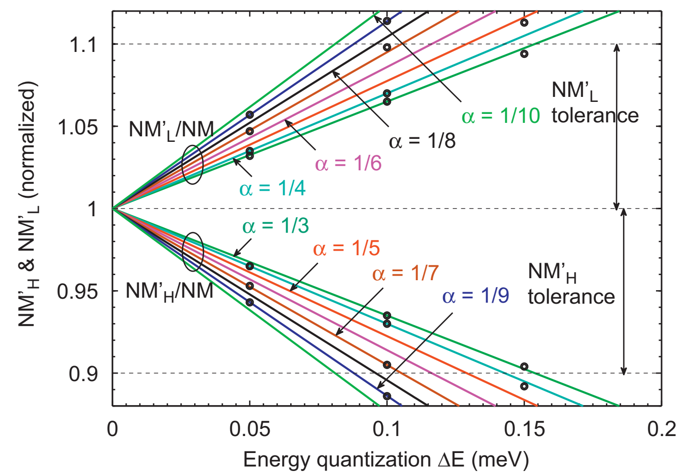


Fig. 8. Variation of normalized noise margins NM'_H/NM and NM'_L/NM of the SET inverter with energy quantization ΔE for different $\alpha = C_T/C_G$ ratios at constant $V_{DD} = 20\,\mathrm{mV}$ bias. The symbols represent simulated data while solid lines indicate the results predicted by the model (noise margin tolerance is taken as 10% of the orthodox value).

SET logic circuit can withstand before the noise margin falls below a specific tolerable value. Equating the relation for noise margin with any specified value of noise tolerance (say 'x%'), we get

$$NM'_H = NM - 2\left(\frac{\alpha^2+\alpha+1}{2\alpha^2+\alpha+1}\right)\frac{\Delta E_{TH}}{e} = NM(1-x) \quad (20)$$

$$NM'_L = NM + 2\left(\frac{\alpha^2+\alpha+1}{2\alpha^2+\alpha+1}\right)\frac{\Delta E_{TH}}{e} = NM(1+x) \quad (21)$$

Putting the expression of orthodox noise margin NM from Eq. (13) into Eqs. (20) and (21) we finally obtain

$$\Delta E_{TH} = \frac{ex\alpha(1-\alpha)V_{DD}}{2(\alpha^2+\alpha+1)} \quad (22)$$

The optimal $\alpha = C_T/C_G$ ratio of the SET inverter circuit for which the maximum robustness can be achieved is calculated by maximizing Eq. (22). Now solving $\partial\Delta E_{TH}/\partial\alpha = 0$ it is found that the condition for achieving maximum robustness against energy quantization effects occurs at $\alpha = (\sqrt{3}-1)/2 = 0.366$ and the maximum quantization threshold $\Delta E_{TH_{max}}$ an SET logic circuit can tolerate is

$$\Delta E_{TH_{max}} = \Delta E_{TH}\Big|_{\alpha=0.366} \approx \frac{exV_{DD}}{13} \quad (23)$$

Eq. (22) is plotted in Fig. 9, where it is shown that the SET inverter can withstand the maximum $\Delta E_{TH_{max}}$ of $exV_{DD}/13$ at the optimum C_T/C_G ratio of 0.366. It is worth noting that in our earlier work [12] we have shown that $C_T/C_G = 1/3$ design criteria also provides maximum robustness against background charge and device parameter variation. On the other hand, for a given bias V_{DD} and ΔE, the α value, for which one can get maximum noise margins, can be obtained from the relations $\partial NM'_{H_{max}}/\partial\alpha = 0$ and $\partial NM'_{L_{max}}/\partial\alpha = 0$ as

$$\alpha(\Delta E)|_{NM'_{max}} = \left[\pm 1 + \sqrt{\left(\frac{eV_{DD}}{\Delta E}\right)^2 + 1 \mp \frac{3}{2}\left(\frac{eV_{DD}}{\Delta E}\right)} - \frac{1}{2}\left(\frac{eV_{DD}}{\Delta E}\right)\right] \Big/ \left[\frac{3}{2}\left(\frac{eV_{DD}}{\Delta E}\right) \mp 1\right] \quad (24)$$

Here $(+,-,-)$ sequence is used for $NM'_{H_{max}}$ and $(-,+,+)$ sequence is used for $NM'_{L_{max}}$. Eq. (24) is plotted in Fig. 10 which shows that

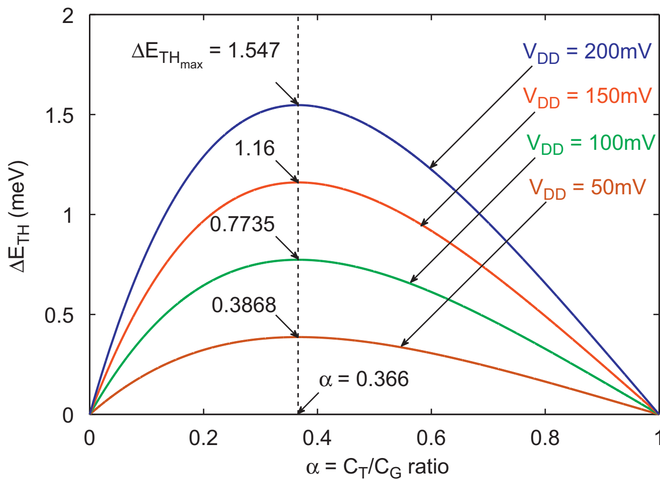


Fig. 9. Variation of quantization threshold ΔE_{TH} as a function of $\alpha = C_T/C_G$ ratio for a noise tolerance of 10% of the orthodox noise margin (i.e. $x = 0.1$). Note that $(C_G + C_T)$ value is decreased (considering SET devices with smaller dimensions) proportionately with increase in V_{DD}.

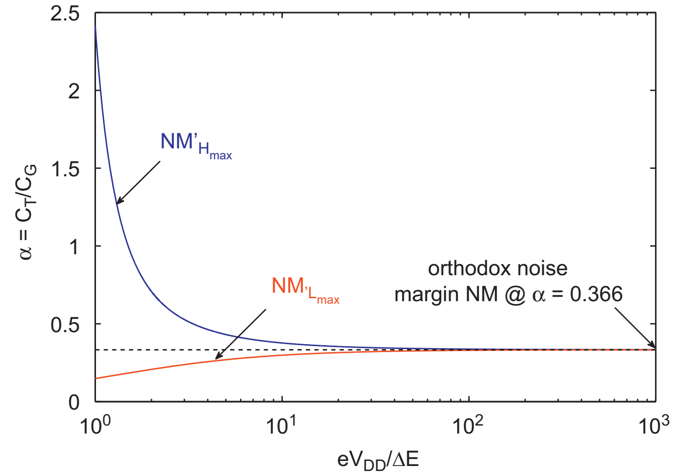


Fig. 10. Variation of $\alpha = C_T/C_G$ ratio as a function of the ratio $eV_{DD}/\Delta E$, indicating the value of α necessary at a given bias V_{DD} and energy quantization ΔE to obtain maximum noise margins.

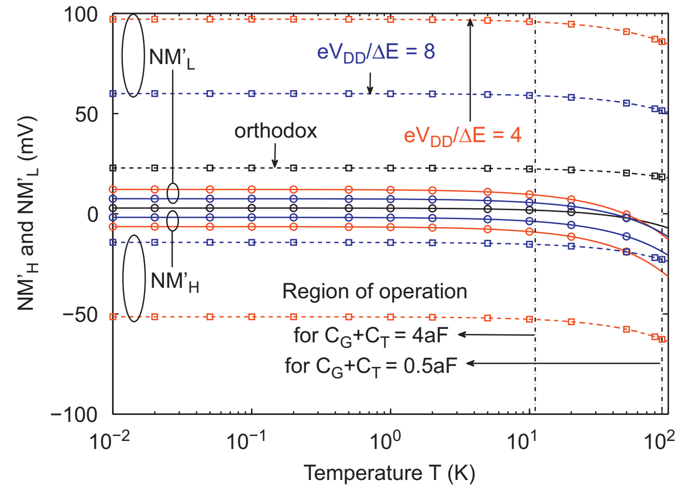


Fig. 11. Influence of temperature on the noise margins of the SET inverter logic for various energy quantization values ΔE. The solid and the broken lines denote the plots for two different inverters with SETs having $C_G + C_T = 4$ and 0.5 aF and, consequently, the optimal $V_{DD} = -V_{SS} = e/2(C_G + C_T) = 20$ and 160 mV, respectively. For the smaller device, SIMON simulator has been re-tuned with $H = 0.004$ and $W = 0.0001$ (simulated for $\alpha = 1/3$ and $eV_{DD}/\Delta E = 4$ and 8).

for high $V_{DD}/\Delta E$ values the noise margins NM'_H and NM'_L asymptotically merges together at the orthodox noise margin NM and this occurs at $\alpha\sim 0.366$. From this figure it can also be concluded that in presence of energy quantization, it is not possible to optimize both noise margins simultaneously by tuning the α parameter.

4.4. Influence of temperature on noise margin

Fig. 11 shows the influence of temperature T on the absolute noise margins NM'_H and NM'_L of SET inverter logic. The maximum operable temperature for using voltage-state SET-based inverter logic circuits was earlier demonstrated [3,11–13] as $T_{max} < e^2/40k_BC_\Sigma$, which implies $T\sim 11$ and 80 K for $C_\Sigma = 5$ aF (solid lines) and 0.625 aF (broken lines), respectively. As the noise margins do not change with temperature in this operating regime, we have not included the temperature term in the proposed model.

5. Conclusion

Using analytical models and Monte Carlo simulation the effects of energy quantization on single electron transistor device and logic inverter is studied. It is observed that energy quantization in SET island mainly changes the Coulomb blockade region and the drain current of SET devices and thus it affects the noise margin, power dissipation, and the propagation delay of SET inverter. Including energy quantization term a new noise margin model for SET inverter is proposed and validated against Monte Carlo simulation. This noise margin model is then used to study the robustness of the SET inverter against energy quantization effects. It is found that SET inverter designed with $C_T : C_G \sim 1/3$ offers the maximum robustness against energy quantization and the maximum tolerable value of energy quantization is found to be $(exV_{DD}/13)$eV for x% tolerance over the orthodox noise margin.

Appendix

Energy quantization shifts the transfer characteristics towards the right. One can simplify the calculations by shifting the origin of the inverter transfer characteristics (which was at $V_{IN}=0$ in the orthodox model), to $V'_{IN}=V_{IN}-\Delta E/e$. Then starting with the transfer characteristics of a typical voltage-state SET inverter, given by [3,12]

$$V_{OUT}^3 + A_2V_{OUT}^2 + A_1V_{OUT} + A_0 = 0 \tag{25}$$

As the order of the terms V_{OUT}^3, $A_2V_{OUT}^2$, and A_1V_{OUT} in Eq. (25) are 10^{-9}, 10^{-6}, and 10^{-3}, respectively, neglecting V_{OUT}^3 and $A_2V_{OUT}^2$ in Eq. (25), one arrives at the linear equation $A_1V_{OUT}+A_0=0$ as followed in Ref. [12]. Including the energy quantization term ΔE, the coefficients A_0 and A_1 change from the standard orthodox forms [3,12] into

$$A'_1 = A_1 - \frac{e^2}{4C_T(C_G+C_T)^3} \times \left[\frac{2C_G\Delta E(C_G^2-C_T^2)}{e^2} + \frac{4C_G^2\Delta E^2(C_G+C_T)^2}{e^4}\right] \tag{26}$$

$$A'_0 = A_0\left[1 - \frac{2C_G(C_G+C_T)\Delta E}{e^2C_T}\right] \tag{27}$$

Using Eqs. (26) and (27) in equation $A'_1V'_{OUT}+A'_0=0$ one obtains

$$V'_{OH} = C_GV_{DD}\left[\frac{C_T-2C_G(C_G+C_T)\Delta E/e^2}{C_G^2+C_GC_T+2C_T^2}\right] \tag{28}$$

The slope of the transfer characteristics in the transition region is given by

$$\frac{\partial V_{OUT}}{\partial V_{IN}} = -\frac{C_G}{C_T} = \frac{V'_{OH}}{V'_{IL}-\Delta E/e} \tag{29}$$

Using this slope formulation one can obtain the expression for V'_{IL} as given below:

$$V'_{IL} = \Delta E - \left[C_TV_{DD}\frac{C_T-2C_G(C_G+C_T)\Delta E/e^2}{C_G^2+C_GC_T+2C_T^2}\right] \tag{30}$$

Proceeding similarly for V_{OL} and V_{IH} one obtains

$$V'_{OL} = -C_GV_{DD}\left[\frac{C_T+2C_G(C_G+C_T)\Delta E/e^2}{C_G^2+C_GC_T+2C_T^2}\right] \tag{31}$$

$$V'_{IH} = \Delta E + \left[C_TV_{DD}\frac{C_T-2C_G(C_G+C_T)\Delta E/e^2}{C_G^2+C_GC_T+2C_T^2}\right] \tag{32}$$

Then the NM'_H and NM'_L are derived from their definition using Eqs. (28)–(32),

$$NM'_H \triangleq V'_{OH} - V'_{IH} = V_{OH}(1-\alpha) - V_{OH}\left(2+\frac{1}{\alpha}+\alpha\right) + \frac{\Delta E}{e} \tag{33}$$

$$NM'_L \triangleq V'_{IL} - V'_{OL} = V_{OH}(1-\alpha) + V_{OH}\left(2+\frac{1}{\alpha}+\alpha\right) + \frac{\Delta E}{e} \tag{34}$$

Eqs. (18) and (19) are derived from Eqs. (33) and (34) by putting the value of V'_{OH} from Eq. (11) into Eqs. (33) and (34).

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