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Drive current boosting of n-type tunnel FET with strained SiGe layer at source

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Abstract

Though silicon tunnel field effect transistor (TFET) has attracted attention for sub-60 mV/decade subthreshold swing and very small OFF current (I_{OFF}), its practical application is questionable due to low ON current (I_{ON}) and complicated fabrication process steps. In this paper, a new n-type classical-MOSFET-alike tunnel FET architecture is proposed, which offers sub-60 mV/decade subthreshold swing along with a significant improvement in I_{ON}. The enhancement in I_{ON} is achieved by introducing a thin strained SiGe layer on top of the silicon source. Through 2D simulations it is observed that the device is nearly free from short channel effect (SCE) and its immunity towards drain induced barrier lowering (DIBL) increases with increasing germanium mole fraction. It is also found that the body bias does not change the drive current but after body current gets affected. An I_{ON} of $\approx 0.58\,mA/\mu m$ and a minimum average subthreshold swing of 13 mV/decade is achieved for 100 nm channel length device with 1.2 V supply voltage and 0.7 Ge mole fraction, while maintaining the I_{OFF} in fA range.

Keywords: Band-to-band tunneling; Subthreshold swing; Gated p–i–n diode; Tunnel field effect transistor (TFET); Device simulation

1. Introduction

The switching characteristics of the metal oxide semiconductor field effect transistor (MOSFET) have degraded considerably over the years due to relentless scaling. The subthreshold swing (S) of the MOSFET, which determines its switching characteristics and OFF current (I_{OFF}) is un-scalable. Due to the drift-diffusion mode of carrier transport, the S in a MOSFET is theoretically limited to a value of 60 mV/decade at the room temperature. In fact, due to various short channel effects (SCEs), punchthrough, etc., the actual value of S in the present day MOSFET is much higher, which has resulted in an increase of I_{OFF} from generation to generation and thus became a major concern for low-standby power (LSTP) applications. One therefore needs to explore novel device architectures which use other mode of carrier transport (i.e., impact ionization [1], interband tunneling [2–14], etc.) in order to achieve sub-60 mV/decade values of S. The impact ionization MOSFET (I-MOS) [1] appeared to be very promising due to its near ideal switching characteristics. However, due to problems like threshold voltage (V_{TH}) shifts caused by hot carrier injection, non-rail to rail voltage swings and high operating voltage requirements, it failed to meet the ITRS [15] requirements for LSTP application.

The tunnel field effect transistor (TFET) with perfect saturation in the output characteristics has shown a lot of promise for achieving better scaling without severe SCEs [6]. Many variants of the TFET have been proposed till date. Among them, the vertical channel tunnel FET with a strained pseudomorphic δ_{p^+} SiGe layer has been the most discussed structure. Due to its complex fabrication steps, routing (layouting) and packaging (not compatible with classical CMOS), Vertical channel TFET does not appear to be practically applicable for LSTP applications. To overcome above difficulties non-Si lateral Tunnel FET has been proposed by Baba [3] and Si lateral Tunnel FET has been proposed by Reddick [4], which enjoys CMOS compatible process steps. However, inspite of excellent

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subthreshold swing and high I_{ON}/I_{OFF} ratio, the very low I_{ON} is the main issue with this device. Recently, ON current improvement in this lateral structure has been reported using high-κ gate dielectric in a double gate structure [16]. However, it does not take into account the mobility degradation related to high-κ material, gate dielectric breakdown due to high field across the very thin high-κ material and fabrication issues related to high-κ material involved.

In this work, we propose a new classical-MOSFET-alike n-type tunnel FET architecture, which offers sub-60 mV/decade subthreshold swing with a significant improvement in I_{ON}. The enhancement in I_{ON} is achieved by introducing a thin strained SiGe layer on top of the silicon source. With the help of TCAD simulations, we have demonstrated that the proposed device is naturally immune to SCE and can be fabricated with standard CMOS process steps. It is observed that the body bias does not affect the drain current but the body current gets affected. Another original finding is that the introduction of strained SiGe layer makes the device immune to drain induced barrier lowering (DIBL) effect and the I_{ON} increases exponentially with Ge mole fraction (x). It is noted that if proposed architecture is coupled with high-κ material (as proposed in [16]) additional boost in drive current can be achieved with a thicker gate dielectric.

2. Device structure and working principle

The device being investigated is a lateral n-type tunnel FET with a strained SiGe layer on the top of the source. The tunnel FET is a gated reverse biased p^+-p-n^+ structure which uses the principle of gate controlled band to band tunneling (BTBT) for its operation. The proposed device is shown in Fig. 1. To operate the device, the p^+ source is grounded, and positive voltage (1 V) is applied to the n^+ drain with a positive sweep at gate. The working principle of conventional (without strained SiGe) TFET and band diagrams are shown in Fig. 2. In the absence of a gate voltage (non-conducting region), the tunneling barrier

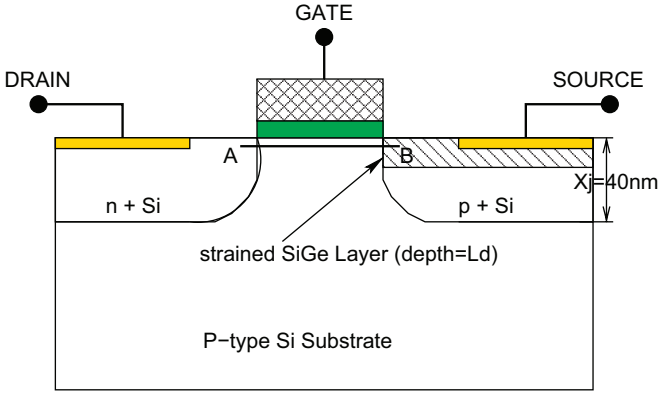

Fig. 1. Schematic of the proposed n-type TFET structure with strained SiGe layer at source. For all simulations, $t_{ox} = 2$ nm, drain doping (n^+) = 5×10^{19} and source doping (p^+) = 1×10^{20} are used.

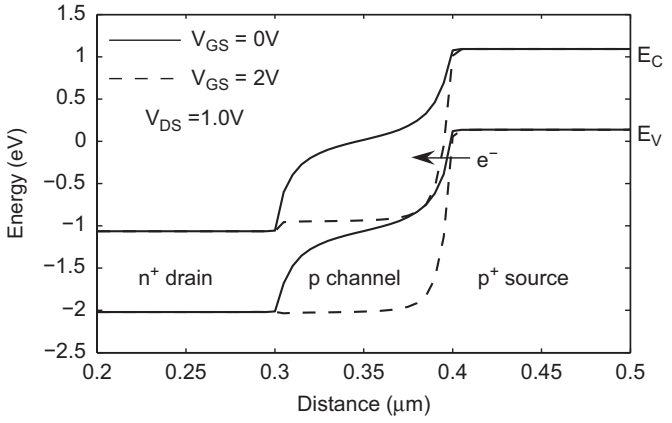

Fig. 2. Simulated band diagrams (along the cut section A–B in Fig. 1) of the n-type conventional (without strained SiGe) TFET in non-conducting and conducting regions. The large reverse biased barrier insures extremely low I_{OFF}.

width is large enough to give extremely small current (I_{OFF}). However, on application of positive gate voltage, the bands in the intrinsic (lowly doped) region are pulled downwards and a tunneling barrier is created between source and channel. Due to the reduction in tunneling width and electric fields produced, zener tunneling of electrons takes place from the valance band of the source to the conduction band of the channel and the device turns ON. One should note that this behavior is analogous to NMOS in the CMOS technology. For a tunnel FET, the ON current is proportional to the electron/hole transmission probability $T(E)$ in the BTBT mechanism, which is given by [17]:

$$T(E) = \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar(E_g+\Delta\Phi)}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{ox}t_{Si}}\right)\Delta\Phi, \quad (1)$$

where m^* is the carrier effective mass, e is the electron charge, E_g is the bandgap, $\Delta\Phi$ is the energy range over which tunneling can take place, and t_{ox}, t_{Si}, ε_{ox} and ε_{Si} are the oxide and silicon film thickness and dielectric constants, respectively. This equation shows decreasing oxide thickness (t_{ox}) [18], increasing oxide dielectric constant (ε_{ox}), and reducing bandgap (E_g), will enhance the performance of the device. Boucart and Ionescu [16] have proposed the use of high-κ materials as the gate dielectric (high ε_{ox} in Eq. (1)) in order to increase ON current (I_{ON}). In this work, I_{ON} enhancement has been done by modulating the bandgap (E_g) by using a strained SiGe layer at the source end and varying its Ge mole fraction (x). As the electron/hole effective mass m^* does not change too much with mole fraction (x), its impact on I_{ON} could be ignored.

The device performance is sensitive to the doping concentration of source and abruptness of doping profile at source-channel [9]. The doping of source, substrate and drain regions chosen to optimize I_{ON}, respectively, are 1×10^{20}, 1×10^{16} and 5×10^{19} cm^{-3}. Device performance is very sensitive to gate work function as reported in[18],

but we have used n^+ polysilicon compatible to CMOS process flow for gate material. A constant oxide thickness ($t_{ox} = 2$ nm) and channel length ($L = 100$ nm) is chosen for all simulations.

3. Simulation models and device parameters

Two-dimensional device simulations are done with field dependent Kane's model [19] available in MEDICI [20] is used to model the BTBT generation and recombination rate. Kane's model has been shown to give a good match for BTBT in silicon based tunnel transistors at both high and low temperatures [4]. Since the source region is heavily doped, and tunneling is a strong function of bandgap, the bandgap narrowing model (BGN) is also included in the simulations. Fermi Dirac statistics, although they are computationally less efficient, are used instead of Boltzmann approximations for the same reason. The BTBT model in Medici is configured in such a way that it uses the average tunneling field while solving the pre-exponential and the path integral field while solving the exponential in the tunneling rate. Also a recursive refinement procedure is used that further improves the accuracy of the simulations. Nonlocal tunneling is enabled which causes the electrons to be generated at the end of the tunneling path as implied by the tunneling physics.

Unlike the MOSFET, where there is a clear transition between the subthreshold and strong inversion, in TFET the slope (of $\log_{10} I_D$) is an exponential function of V_{GS}. The slope is very steep for lower V_{GS} but becomes less and less steeper as the gate voltage increases. Therefore, the threshold voltage (V_{TH}) cannot be extracted using the standard MOSFET techniques (linear extrapolation, maximum conductance, etc.). Hence, as discussed in [21], V_{TH} is calculated by a constant current method at $I_{VT} = 10^{-7}$ A/μm. The average subthreshold swing is extracted by taking the average between the gate voltage at which the I_D begins to increase and the threshold voltage. This method has been explained in detail earlier by [16,18] and is considered to be a consistent way to define S for TFET. I_{ON} is calculated at $V_{GS} = V_{DS} = 1.2$ V as per the voltages specified by ITRS for LSTP applications at the 65 nm node.

4. Results and discussion

4.1. The strained SiGe layer

As discussed earlier, a strained SiGe layer is introduced at the top of the source in the conventional tunnel FET to achieve an improvement in the ON state current. Fig. 3(a) shows the effect of varying the Ge mole fraction (x) in the equilibrium band diagrams of the proposed device. As expected, the bandgap at the source end reduces as we increase the Ge mole fraction (x). This results in a reduction in the tunneling bandgap and consequently an increase in the transmission probability (Eq. (1)) and drive

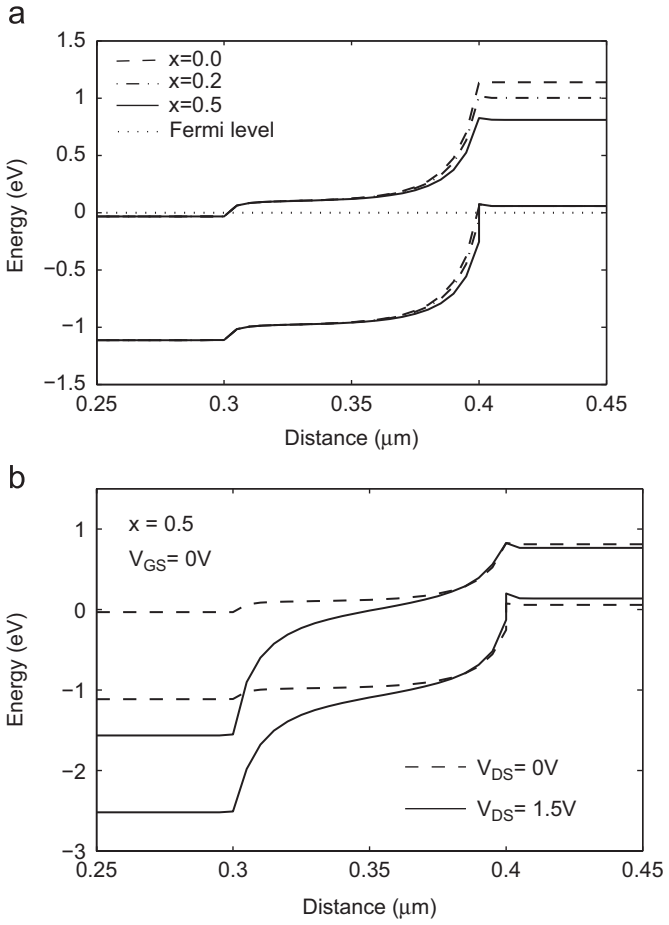

Fig. 3. Simulated band diagrams of the proposed tunnel FET architecture in Fig. 1 along the cut section (A–B). (a) Equilibrium band diagrams of the proposed TFET structure for various values of Ge mole fraction (x). (b) Effect of drain voltage on the device band diagrams. It is seen that the tunneling width remains nearly independent of the applied drain bias. Thus insuring high immunity to DIBL.

current. Fig. 3(b) shows how the bands vary under the effect of drain bias. As can be seen there is negligible change in the tunneling band height and width with increase in V_{DS}.

The transfer and output characteristics of the proposed device are shown in Fig. 4. As expected, in Fig. 4(a) we observe that, the over all drain current and specially the ON current increases as we increase the Ge mole fraction (x). Fig. 4(b) shows the output characteristics of the device. Due to the reverse biased p–i–n structure, the output impedance of the device is very high. This is also seen in the I_{DS} vs. V_{DS} curves where the drain current is almost constant in the saturation region.

According to Eq. (1), we observe in Fig. 5 that, the increase in I_{ON} is exponentially dependent on the reduction in E_g (which reduces linearly with increase in Ge mole fraction (x)). Also, this increase in I_{ON} leads to a reduction in the average subthreshold swing of the device since now the threshold voltage falls in the steeper region of the curve. *I_{ON} of 580 μA/μm, I_{OFF} of 0.52 fA/μm and average S of 13 mV/decade are achieved for $x = 0.7$ with $V_{DD} = 1.2$ V.*

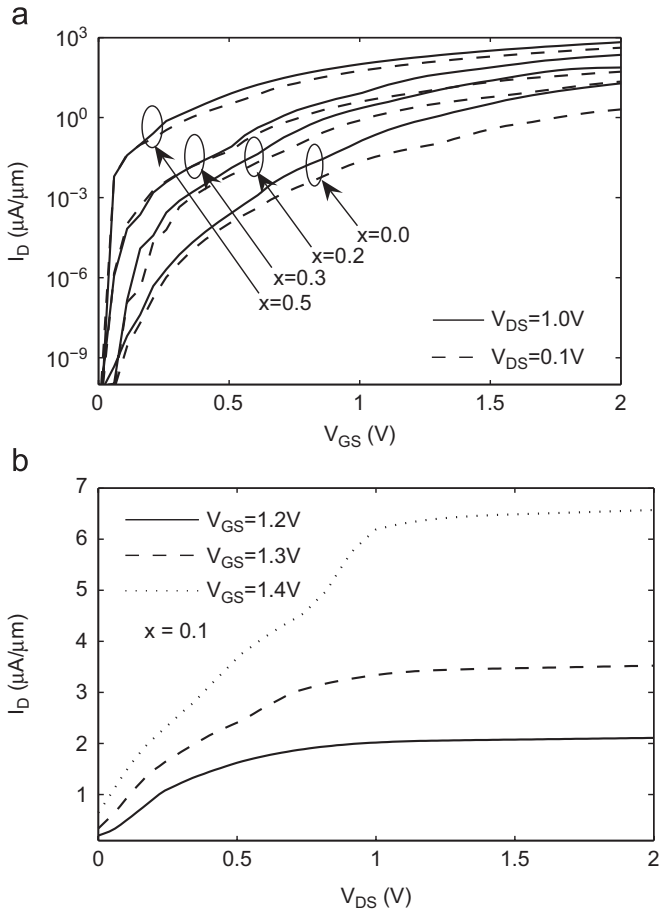

Fig. 4. Simulated device characteristics for the proposed device. (a) Simulated transfer characteristics of the device for various values of Ge mole fraction (x) for linear and saturation V_{DS}. (b) Output characteristics of the TFET with strained SiGe layer at the source end.

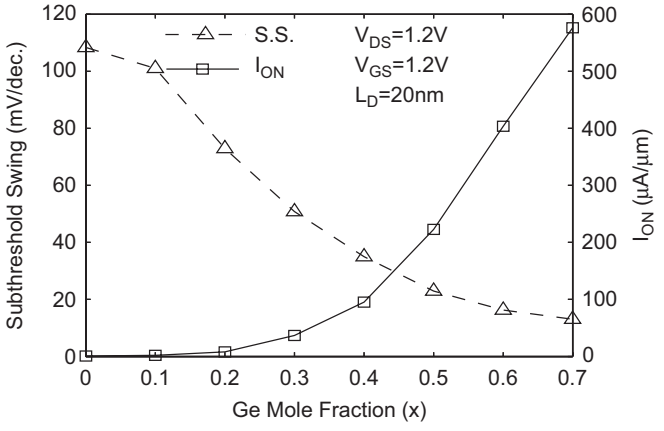

Fig. 5. The average subthreshold swing (S) and I_{ON} vs. x. I_{ON} increases exponentially with x. However, the I_{OFF} remains in the order of fA.

However, enabling the tunneling through gate oxide, gate leakage current of $3.7\,mA/cm^2$ is observed, which is one decade lower than ITRS specs. It should be noted that I_{ON} is matched with ITRS specs with thicker t_{ox}, that enables us lower gate leakage.

4.2. Depth of SiGe layer (L_d)

Proposed TFET is a surface tunneling device and the active region of the device is situated right at the surface near the channel–source junction. From 2D device simulations, it is observed that the band to band generation rate is maximum at the surface and has some practical value only in the top 20 nm layer of the device (Fig. 6). Therefore, it is believed that increase in I_{ON} can be achieved by reducing bandgap only in this 20 nm region right below the surface. This fact is verified in Fig. 7, where we observe that the I_{ON} of the device increases as we increase the depth of SiGe (L_d) layer to 20 nm but does not increase further beyond this value. Any additional increase in the SiGe layer depth only causes an increase in the I_{OFF} of the device. It is also observed in Fig. 7 that the effect of L_d becomes more prominent as the value of the mole fraction (x) is increased.

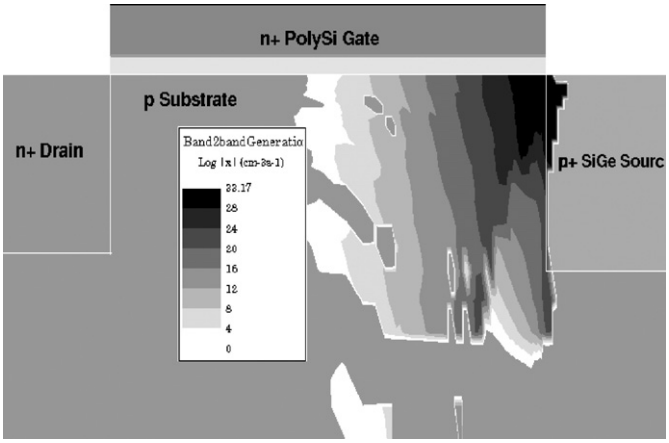

Fig. 6. A zoomed view of the tunneling junction of the TFET. Two-dimensional simulations show that the band to band generation is limited to the top 20 nm layer of the device (when it is biased in the operating region).

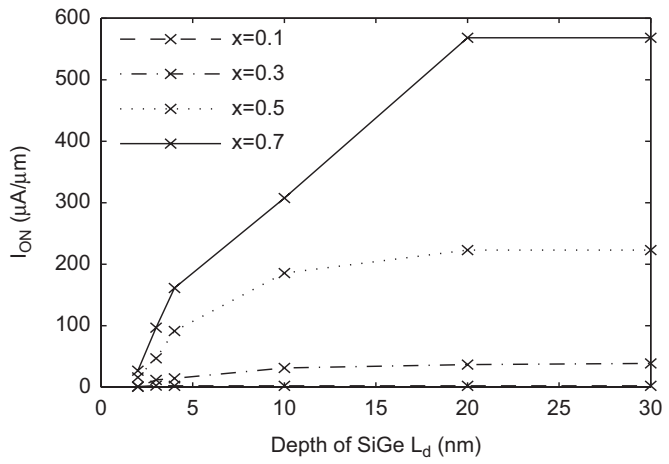

Fig. 7. I_{ON} as a function of the depth of SiGe layer (L_d). I_{ON} increases with an increase in L_d up to a depth of 20 nm. Increasing L_d beyond this value does not help in increasing I_{ON} as it falls beyond the active region of the device.

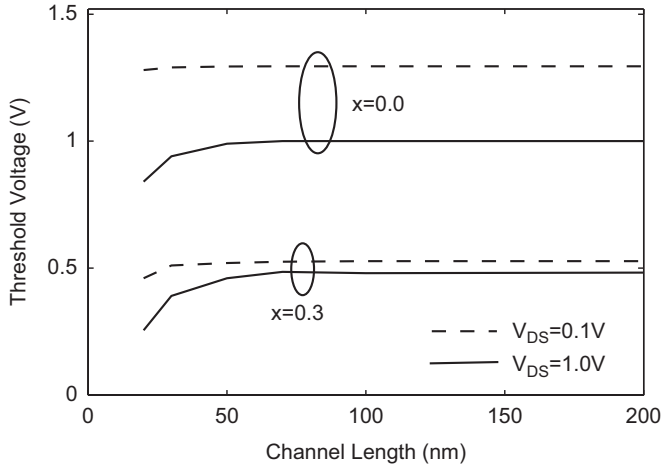

Fig. 8. SCE and DIBL in the proposed device. A suppression of SCE is seen with an increase in x. DIBL also disappears with an increase in x.

4.3. SCE and DIBL

The active region of the TFET is only a very thin region near the surface at the channel source interface. This, along with the large reverse biased barrier, makes the TFET a highly scalable device. It is shown that the device can be scaled up to channel lengths as small as 30 nm without affecting its performance. Fig. 8 shows the effect of channel length and drain bias on the threshold voltage (V_{TH}) of the device. V_{TH} values, which are quite high for $x = 0$, agree well with ITRS requirements [15] for higher values of x. Also, it is observed that there is virtually no DIBL for higher values of x (above $x = 0.3$). This is because, the barrier width (which is directly proportional to the tunneling bandgap) is a much stronger function of x than V_{DS}. Therefore, as we increase the mole fraction (x), the lowering of bandgap by x dominates the lowering of bandgap by V_{DS}.

4.4. Effect of body bias

Fig. 9 shows the effect of body bias on the proposed device characteristics. Unlike MOSFET, both positive and negative body bias turn on either body/drain or body/source diode (forward bias) and generate a significant amount of substrate current. However, due to the difference in the effective forward biases, the magnitude of I_{BULK} would be quite different for positive and negative body voltages. It should be noted that in contrast with MOSFET, body bias does not change the threshold voltage and the drive current of the proposed device.

4.5. High-κ material as gate dielectric

In [16], the use of high-κ materials to improve the I_{ON} of the device has been reported. The thickness of the dielectric material needed to achieve this improvement in I_{ON} is very small (3 nm). It may not be practical to use such thin high-κ dielectric as their breakdown voltages are much smaller compared to SiO_2. However, if the same technology is used with the proposed TFET design, it is possible to achieve

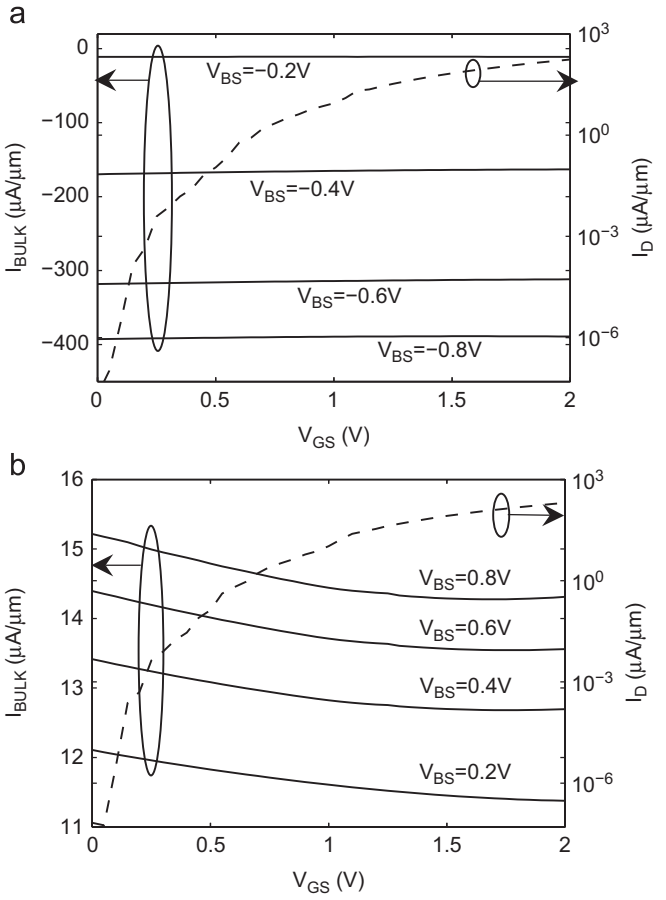

Fig. 9. Effect of body bias on device performance (Ge mole fraction (x) = 0.3, $V_{DS} = 1.0$ V). The $I_D - V_{GS}$ characteristics remain unaltered but the bulk current increases linearly with increase in bulk terminal potential. (a) Effect of negative body bias. (b) Effect of positive body bias.

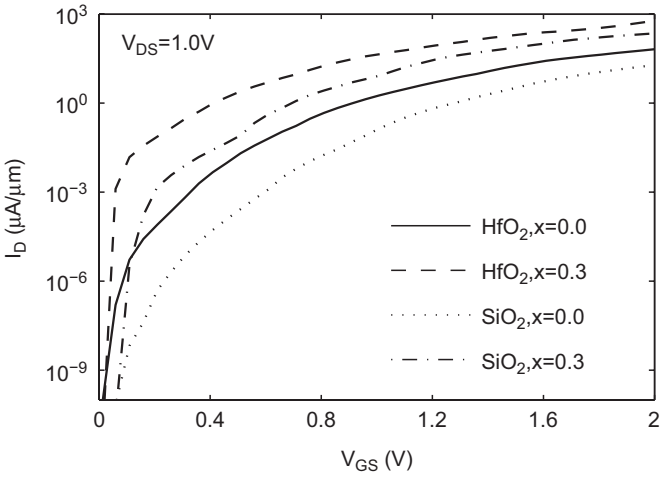

Fig. 10. Combination of high-κ ($\varepsilon = 29$) along with the strained SiGe layer at the source end helps in achieving much better I_{ON} and subthreshold swing for realistic physical thickness. $L_d = 10$ nm, $T_{dielectric} = 5$ nm in this case.

better I_{ON} even for a thicker, more realistic physical dielectric thickness (more than 5 nm). Fig. 10 shows the transfer characteristics comparing the two devices with different dielectric constants (HfO_2 and SiO_2) for two different values of Ge mole fractions. It is seen that a very high I_{ON} (nearly 1 mA/μm) can be achieved if both the techniques are combined.

4.6. Effect of strain on the channel

The reasons behind adding the strained SiGe layer only to the source region are twofold. First, the active region of the device is located only at the source–channel junction and the drain voltage does not play any role in BTBT tunneling. Second, adding SiGe to the drain also would add strain to the channel from both sides. This strain in the channel may increase/reduce the carrier mobility. Therefore, it is very difficult to predict the effect of stress and requires further investigation. In fact the proposed device will operate with same efficiency if we use fully silicon–germanide source instead of strained SiGe layer on the top of a Si source. However, we propose strained SiGe layer source in order to minimize the effect of stress on the silicon channel. The effect of strain on the Si channel is not considered in this work due to non-availability of proper models in the simulator.

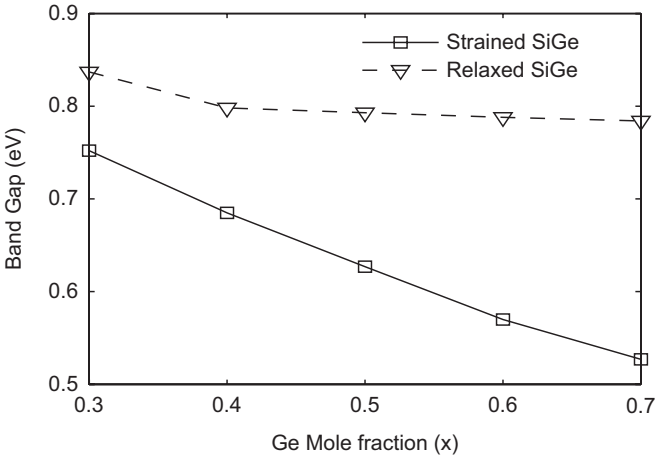

Fig. 11. Band gap of strained SiGe and relaxed SiGe for different values of Ge mole fraction. Strain tends to reduce the band gap and thus helps in improving I_{ON}.

4.7. Effect of strain on SiGe layer

The effect of strain on SiGe bandgap is shown in Fig. 11. The band gap values are extracted from 2D simulations in Medici. It is observed that strain tends to reduce the band gap of the SiGe layer. This further helps in improving the I_{ON} of the device. Thus, it is desirable to have a strained SiGe layer at the source. To obtain 20 nm or more thicker layer of strained SiGe over Si with Ge mole fraction $x = 0.7$ is a challenging technology problem (it can be obtained by growing over relaxed SiGe) [22]. But the same I_{ON} can be obtained with lower Ge mole fraction by decreasing t_{ox} (compromising with gate leakage).

5. Fabrication of the proposed device

One of different possible process flow compatible with standard CMOS process to fabricate the proposed device is shown in Fig. 12, which is the modification of metal gate MOSFET fabrication process proposed in [23]. It involves the following process steps, starting with Si wafer containing thin layer of strained SiGe(~20 nm) on top: (i) shallow

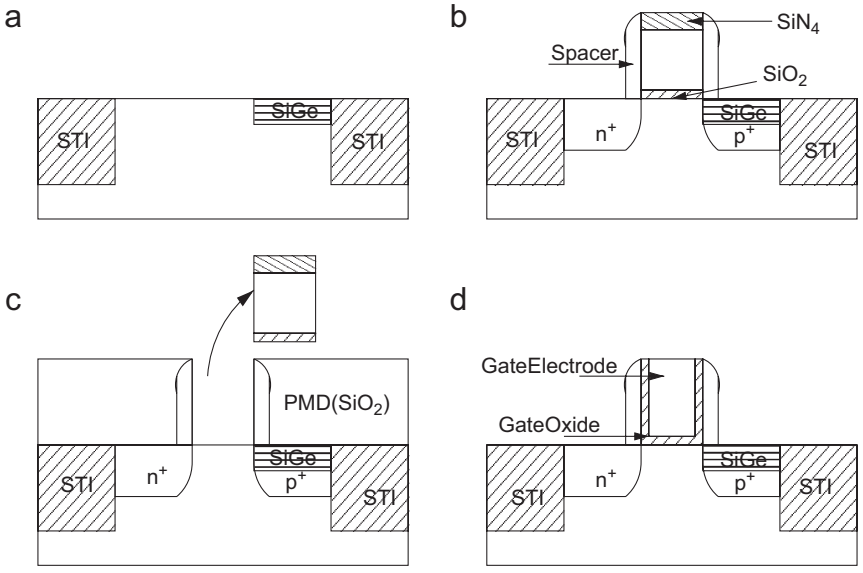

Fig. 12. n-Type tunnel FET fabrication process steps proposed: (a) STI, etch SiGe in drain and channel, grow Si; (b) dummy gate formation, source (p+) and drain (n+) doping, spacer formation; (c) PMD deposition, CMP, remove dummy gate; and (d) clean Si surface with HF treatment, gate stack formation, CMP, remove PMD.

trench isolation (STI) formation, etch SiGe layer in the drain and channel region, grow Si in that region; (ii) dummy gate (Si_3N_4/poly-Si/SiO_2) formation, source and drain region doped with p-type and n-type dopant, respectively, using two separate masks, spacer formation. The dummy gate is used because, due to mask misalignment, the gate is partially doped p+ and hence needs to be replaced by a new gate stack; (iii) deposit pre-metal dielectric (PMD) film (SiO_2), CMP till the Si_3N_4 in dummy gate stack exposed, remove the dummy gate; (iv) Si surface cleaned by HF treatment, grow gate oxide (SiO_2/HK), deposit gate electrode (n^+poly-Si/metal), CMP, remove PMD film (SiO_2).

6. Conclusion

A novel planar silicon tunnel FET architecture with strained SiGe layer at source is proposed and analyzed using 2D device simulations. The proposed device is nearly free of SCE and DIBL and can be scaled upto channel lengths of 30 nm. The proposed device shows orders of improvement in ON current over the conventional TFET with the added advantage of compatibility with CMOS fabrication steps.

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