Performance limits of transition metal dichalcogenide (MX2) nanotube surround gate ballistic field effect transistors

Amretashis Sengupta and Santanu Mahapatra

Citation: J. Appl. Phys. **113**, 194502 (2013); doi: 10.1063/1.4805059
View online: http://dx.doi.org/10.1063/1.4805059
View Table of Contents: http://jap.aip.org/resource/1/JAPIAU/v113/i19
Published by the American Institute of Physics.

Performance limits of transition metal dichalcogenide (MX_2) nanotube surround gate ballistic field effect transistors

Amretashis Sengupta[a] and Santanu Mahapatra
Nano-Scale Device Research Laboratory, Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore 560 012, India

(Received 22 February 2013; accepted 30 April 2013; published online 16 May 2013)

We theoretically analyze the performance of transition metal dichalcogenide (MX_2) single wall nanotube (SWNT) surround gate MOSFET, in the 10 nm technology node. We consider semiconducting armchair (n, n) SWNT of MoS_2, $MoSe_2$, WS_2, and WSe_2 for our study. The material properties of the nanotubes are evaluated from the density functional theory, and the ballistic device characteristics are obtained by self-consistently solving the Poisson-Schrödinger equation under the non-equilibrium Green's function formalism. Simulated ON currents are in the range of 61–76 μA for 4.5 nm diameter MX_2 tubes, with peak transconductance ~175–218 μS and ON/OFF ratio ~0.6×10^5–0.8×10^5. The subthreshold slope is ~62.22 mV/decade and a nominal drain induced barrier lowering of ~12–15 mV/V is observed for the devices. The tungsten dichalcogenide nanotubes offer superior device output characteristics compared to the molybdenum dichalcogenide nanotubes, with WSe_2 showing the best performance. Studying SWNT diameters of 2.5–5 nm, it is found that increase in diameter provides smaller carrier effective mass and 4%–6% higher ON currents. Using mean free path calculation to project the quasi-ballistic currents, 62%–75% reduction from ballistic values in drain current in long channel lengths of 100, 200 nm is observed. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4805059]

I. INTRODUCTION

Since the demonstration of monolayer MoS_2 metal oxide semiconductor field effect transistors (MOSFET) device and logic,[1,2] transition metal dichalcogenides (MX_2: where M stands for transition metal and X for chalcogen) have garnered lot of attention of the MOS device community.[3–5] Such materials have a distinct advantage over graphene due to their non-zero band gap in their monolayer form, which is mandatory for switching applications.[1,2] However, monolayer channels like graphene or 2-D MoS_2 are susceptible to crumpling and rolling,[6,7] which can significantly limit the performance of such devices. Also in case of nanoribbons of graphene or MX_2, edge effects pose a serious threat to device performance.[8]

However, nanotubes of MX_2 materials are more stable compared to their monolayer counterparts and have been successfully fabricated experimentally.[9–12] Thus despite the ease of integration of monolayer MX_2 into planar MOSFET technology,[1,2,13] there remains need for study on multi-gate architectures based on MX_2 nanotubes. The superior electrostatic control of the gate terminal over the channel in multi-gate MOSFET has provided an efficient way of device scaling beyond the 22 nm technology node.[14,15] Of these, the surround gate or gate-all-around architecture is considered as a potential replacement of the planar silicon MOS in the near future.[14,15] For the 10 nm technology node, surround gate MX_2 nanotube MOSFETs could prove useful. Though much work has been done on MX_2 nanotubes experimentally[9–12] and theoretically,[16–18] not much study has been conducted on MOSFET applications of MX_2 nanotubes.

In our studies, we consider semiconducting armchair (n, n) single wall nanotube (SWNT) of MoS_2, $MoSe_2$, WS_2, and WSe_2 as the channel material in a 10 nm channel length, surround gate (SG) MOSFET. The reason for choosing these materials for our study is that stable SWNTs of these materials have been demonstrated experimentally.[9–12] We consider 4.5 nm diameter SWNTs of the said materials, surrounded co-axially with high-k HfO_2 gate dielectric. We take heavily (n^+) doped semi-infinite MX_2 NT as our source and drain, and the terminals are assumed metallic. We evaluate the material properties of the SWNTs like bandstructure and electron effective mass, from Density Functional Theory (DFT). Thereafter, constructing the effective mass Hamiltonian of the system, we proceed to solve the Poisson and the Schrödinger equations self-consistently under the non-equilibrium Green's function (NEGF) approach. We study the MX_2 nanotube FETs for their performance in terms of drive currents, ON/OFF ratio, transconductance, intrinsic delay time, and cut-off frequencies. We also study (n, n) SWNT of varying diameters for their device performance. Since the channel length considered is only 10 nm, we have assumed the carrier transport in our devices to be fully ballistic in nature. Further using the backscattering coefficient method, performance for quasi-ballistic channel lengths is also studied.

II. METHODOLOGY

Fig. 1, shows the schematic diagram of the surround gate MX_2 SWNT MOSFET, on which our device simulations are performed. A 10 nm long SWNT of MX_2 material

[a]Author to whom correspondence should be addressed. Electronic mail: amretashis@dese.iisc.ernet.in. Fax: +91-80-23600808.

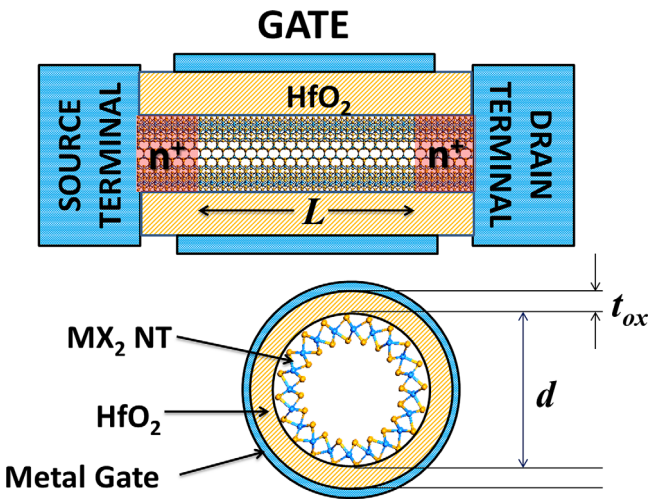

FIG. 1. Device schematic (not to scale) of the surround gate MX_2 nanotube MOSFET considered in our studies.

(MoS_2, $MoSe_2$, WS_2, and WSe_2) is considered as the channel. The diameter of the nanotube is assumed 4.5 nm, in consistency with recently reported MX_2 nanotubes.[9–12] In our studies, we have later explored smaller and larger diameter (2.5, 3.5, and 5 nm) nanotubes as well for investigating their device performance. HfO_2 is taken as the coaxial gate dielectric having 2.5 nm thickness. We take heavily (doping concentration 3–5 $\times 10^{19}$ /cm^3) doped semi-infinite MX_2 NT as our source and drain, and the terminals are assumed metallic. Such doping levels in the source and drain allow good alignment of the source Fermi-level to that of the device and gives superior performance compared to metallic source/drain Schottky barrier (SB) FETs.[5,13] Such device dimensions are also consistent with the surround gate architectures for the 10 nm nodes.[14,15]

In our study, we first evaluate the material properties of the MX_2 SWNTs. For this purpose, we employ DFT in QuantumWise Atomistix ToolKit (ATK).[19] The Localized Density Approximation (LDA) exchange correlation with a Double Zeta Polarized (DZP) basis is used with a mesh cut-off energy of 75 Ha.[20] The Pulay-mixer algorithm is employed as iteration control parameter with tolerance value of 10^{-5}. The maximum number of iteration step is set to 100. We use a $1 \times 1 \times 16$ Monkhorst-Pack k-grid mesh for our simulations.[21] All the DFT simulations are performed by relaxing the nanotube structures by optimizing the positions by a Broyden–Fletcher–Goldfarb–Shanno (BFGS) (Ref. 22) Quasi-Newton optimization method in ATK with maximum force 0.05 eV/Å and cell optimization performed with maximum stress of 0.05 eV/Å^3.

From the *ab-initio* studies, the bandstructure and the effective mass of the MX_2 SWNTs are evaluated. From these computed electrical parameters, we set up the effective mass Hamiltonian (H) of the channel.[23,24] Thereafter, we proceed to solve the-Poisson Schrödinger equation of the system (described in Fig. 1) self-consistently under the NEGF formalism.[23,24] Setting up the self-energy matrices Σ_S and Σ_D for the source and drain contacts, the Green's function G is constructed as

$$G(E) = [EI - H - \Sigma_S - \Sigma_D]^{-1}. \quad (1)$$

In Eq. (1), I is the identity matrix. It is notable that here we consider the transport to be fully ballistic and therefore no scattering energy matrix has been incorporated into the Green's function.[24] From Eq. (1), parameters like the broadening matrices Γ_S and Γ_D and the spectral densities A_S and A_D are evaluated using the following relations:

$$\Gamma_{S,D} = i[\Sigma_{S,D} - \Sigma_{S,D}^{\dagger}], \quad (2)$$

$$A_{S,D}(E) = G(E)\Gamma_{S,D}G^{\dagger}(E). \quad (3)$$

The density matrix $[\Re]$ used to solve the Poisson equation is given by

$$[\Re] = \int_{-\infty}^{\infty} \frac{dE}{2\pi}[A(E_{k,x})]f_0(E_{k,x} - \eta), \quad (4)$$

where $A(E_{k,x})$ is the spectral density matrix, $E_{k,x}$ is the energy of the conducting level, η being the chemical potential of the contacts, and f_0 is the Fermi function.

For the Poisson solver, we follow the methodology similar to Guo *et al.*[25] and Ren[26] and consider the linearized finite difference form of the Poisson equation at a grid point (z_i, r_j) in the 2-D mesh as

$$\frac{r_{j-1} + r_j}{2}\frac{a}{b}(U_{i,j-1} - U_{i,j}) + \frac{r_{j+1} + r_j}{2}\frac{a}{b}(U_{i,j+1} - U_{i,j}) + r_j\frac{a}{b}(U_{i+1,j} - U_{i,j}) + r_j\frac{a}{b}(U_{i-1,j} - U_{i,j}) = -\frac{qan_{tot}}{2\pi\varepsilon_0}, \quad (5)$$

where a and b are the mesh spacing in the transverse (along the axis) and the radial directions of the NT, $U_{i,j}$ is the potential expressed as the vacuum energy level minus the work function of the intrinsic NT. The value of $U_{i,j}$ at the surface of the NT is equal to the mid-gap energy. n_{tot} is the electron charge density which is non-zero only for grid points on the NT surface, which is calculated (self-consistently in the Poisson-NEGF solver) from the density matrix $\Re$. In Eq. (5), we have considered the grid point to be in air and hence the dielectric constant is ε_0. However, depending upon the location of the grid point (on the NT surface, in the gate dielectric), it can assume the dielectric constant of that particular region. For grid points situated at the interfaces of different materials, different dielectric constants are used at the volume surfaces lying at different regions of the interface.[25] The boundary conditions imposed on the radial direction are the Dirichlet conditions and that in the transverse direction are Neumann in nature.[25,26]

The carrier densities evaluated from the NEGF formalism are put into the Poisson solver to evaluate a more accurate guess of the self-consistent potential U_{SCF} and the same is used to evaluate a better n_{tot}. The converged values are used to evaluate the transmission matrix $T(E)$ as

$$T(E) = Trace[A_S\Gamma_D] = Trace[A_D\Gamma_S]. \quad (6)$$

From this, the ballistic drain current is easily evaluated as[23,24]

$$I_D = \left(\frac{4e}{h}\right)\int_{-\infty}^{+\infty} T(E)[f_S(E_{k,x}-\eta_S) - f_D(E_{k,x}-\eta_D)]dE. \quad (7)$$

In Eq. (6), e is the electronic charge, h is the Planck's constant, f_S and f_D are the Fermi functions in the source and drain contacts. η_S and η_D are the source and drain chemical potentials, respectively. The factor 4 originates from the spin degeneracy and valley degeneracy in MX_2 nanotubes. Equation (6) represents fully ballistic transport in the nanotube FETs which holds good for short channel lengths below 100 nm.[24,25]

The channel conductance is calculated using

$$G_{CH} = \frac{2g_v q^2}{h}\int_{-\infty}^{+\infty} T(E)\frac{\partial f(E)}{\partial E}dE, \quad (8)$$

where g_v is the valley degeneracy, the factor 2 comes from the spin degeneracy, f is the Fermi function.

Most experimentally, fabricated nanotubes of MX_2 have lengths of few hundred nanometers to few microns. Therefore for such longer channel lengths, the transport can no longer be safely assumed ballistic. For such longer channels, we can project the quasi-ballistic currents following a method described by Yoon *et al.*[4] and Alam *et al.*[5] for 2-D channel MOSFETs. We consider a factor Θ to be multiplied with the ballistic currents in Eq. (7) to give the projected current for the long channel devices

$$\Theta = \frac{\lambda_{max}}{L + \lambda_{max}}, \quad (9)$$

where L is the channel length and λ_{max} is the carrier mean free path in the SWNT calculated as

$$\lambda_{max} = \frac{(2k_BT)^{3/2}}{q\mu}\frac{f_0(\eta_S - E_C)}{\Im_{-1/2}(\eta_S - E_C)}. \quad (10)$$

In Eq. (10), E_C is the top of the conduction band energy in the channel, which is evaluated from the maxima of the self-consistent potential in the channel, $\Im_{-1/2}$ is the 0-D Fermi integral of order $-1/2$, μ is the carrier mobility. For short channel lengths, $\lambda_{max} \gg L_{Ch}$ and therefore $\Theta \to 1$ which is the purely ballistic case. It is worth mentioning that this method of projecting quasi-ballistic currents is an approximate one and does not strictly incorporate all possible scattering events in longer channels. However, it is a good indicator of current degradation for longer channel devices.

III. RESULTS AND DISCUSSIONS

From our DFT studies, we calculate the bandstructures of the various MX_2 (n, n) SWNTs of 4.5 nm diameter as shown in Fig. 2. In our studies, we exclude WTe_2 as so far there are no reports of stable "h" polytype WTe_2 sheets or nanotubes fabricated experimentally. The DFT studies for the $MoTe_2$ SWNTs (not presented here) displayed a smaller indirect gap than the direct gap. Thus, it may not be correctly

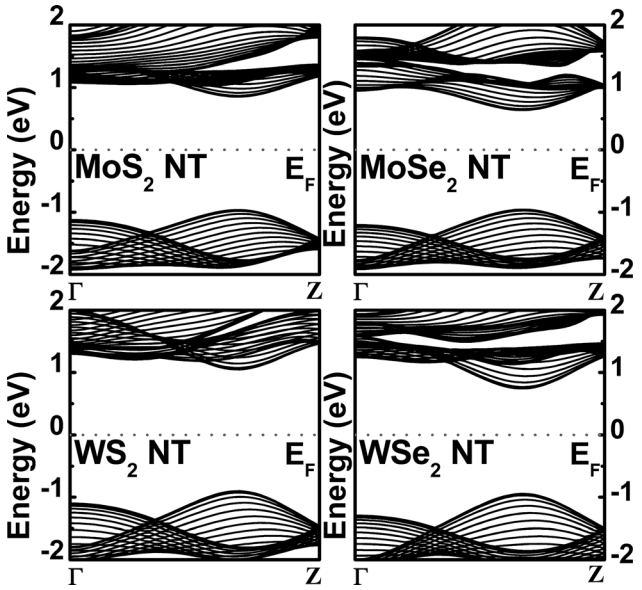

FIG. 2. Calculated band structure of the various (n, n) MX_2 SWNTs from our *ab-initio* simulations.

treated under the present NEGF formalism used in the study, and hence we do not include $MoTe_2$ nanotubes in the following discussion. We see that all the nanotubes show a direct band gap at about 2/3 way in between the Γ point and the Z point of the Brillouin zone.

The calculations show value of direct band-gaps of 1.78, 1.60, 1.93, and 1.67 eV for the MoS_2, $MoSe_2$, WS_2, and WSe_2 nanotubes, respectively. The value of band gap seems to increase slightly with increasing diameter. The variation in band-gap with SWNT diameter is given in Fig. 3(a). Here we see for a 2.5 nm MX_2 SWNT, the band gap values are 1.73, 1.51, 1.89, and 1.63 eV for the MoS_2, $MoSe_2$, WS_2, and WSe_2 nanotubes, respectively. This result may appear surprising initially, as the increase in quantum confinement with smaller diameter NTs should increase the energy band gap in general. However, this is a typical behavior of MX_2 NTs as established by various *ab-initio*[16,27] and experimental[28,29] studies by other researchers. The reason for such anomalous behavior has its origin in the lattice distortion induced by wrapping layered structure like 2 H-MX_2 (Ref. 30) due to which the LUMO states in such MX_2 NT change in a manner so that the band-gap decreases with the diameter reduction.[31] Such behavior occurs in MX_2 NTs due to the three different layers of atoms present in a sheet of such a material. As all, the atoms in a graphene sheet are co-planar, hence lattice distortion effects cannot outweigh the quantum confinement and therefore the band-gap increases with diameter reduction.

These values are in good agreement, being slightly (~3%–5%) higher than those reported for MX_2 nanotubes, from density functional tight binding (DFTB) methods.[16] In order to compare our DFT results with experimental data, we calculate the band gap of a 20 nm diameter WS_2 SWNT. The DFT results obtained from ATK using the k-point and pseudopotential settings as described in Sec. II showed a direct band gap of 1.97 eV, which is close to the experimental value of 1.91 eV obtained for 1–2 layer WS_2 nanotubes of diameter

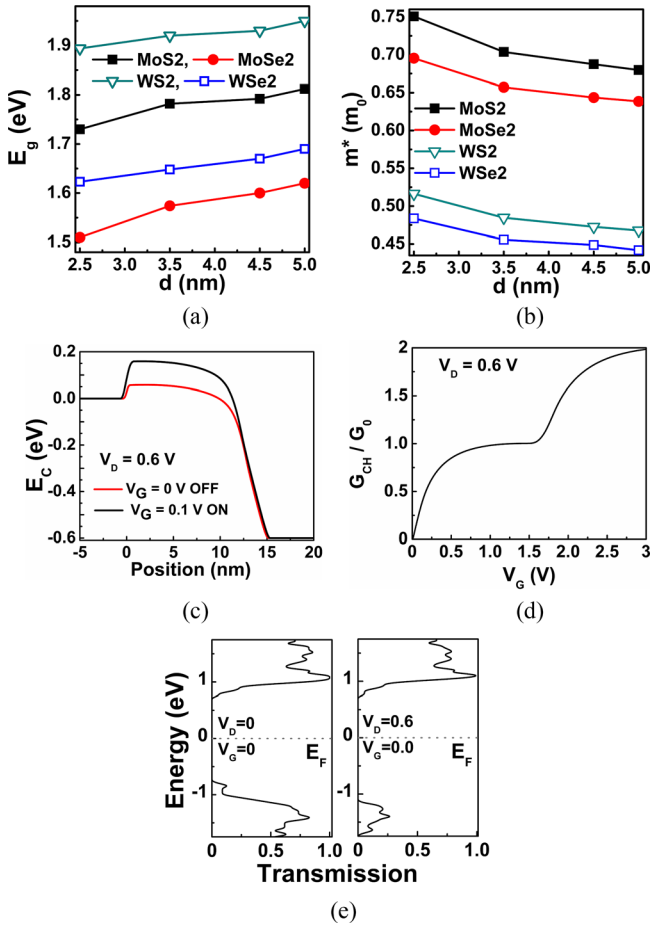

FIG. 3. (a) Variation of direct band gap of (*n*,*n*) MX2 SWNT with nanotube diameter. (b) Variation of electron effective mass with diameter of MX2 SWNT. (c) Conduction band profile of the device for ON and OFF states. (d) Variation of channel conductance with gate bias and (e) transmission spectra under different bias conditions.

17.5–20 nm by Frey *et al.*[28] In Fig. 3(b), we show the variation of the electron effective mass with diameter of the various nanotubes under consideration. Here we see that the tungsten dichalcogenide tubes offer considerably lesser electron effective mass compared to their molybdenum dichalcogenide counterparts, with WSe2 NTs showing the least effective mass. As SWNT diameter increases, the effective mass tends to decrease and for tube diameter of 4.5 nm and more, the rate of this change decreases. For our 4.5 nm diameter tube considered in the device, the effective masses are 0.6874, 0.6436, 0.4725, and 0.4488 m_0 for MoS_2, $MoSe_2$, WS_2, and WSe_2, respectively. The static dielectric constants $\mathrm{Re}[\varepsilon(\omega = 0)]$ for the different NTs were calculated from the simulated optical spectra in ATK. The shape anisotropy of the nanotubes gives rise to two different dielectric constants ε_{zz} and ε_{rr}. As we are solving the Poisson equation by effectively slicing up the device in thin laminar regions in the z direction[25,26] hence ε_{rr} was used as the dielectric constant. Its values are 1.33, 1.21, 1.20, and 1.23 for the MoS_2, $MoSe_2$, WS_2 and the WSe_2 SWNT, respectively. The static dielectric constants did not seem to be significantly affected by diameter variations of the NTs. Using the calculated material properties, we solve the Poisson-Schrödinger equation of our system self-consistently under the NEGF formalism as discussed in Sec. II.

We consider the source and drain are heavily doped with doping concentrations in the range $3–5 \times 10^{19}$ /cm^3. Such doping concentrations provide very good alignment of the source drain Fermi levels to the conduction band edge.[5,13,32,33] For MoS_2 NT for a doping concentration of 3.25×10^{19} /cm^3, the source/drain Fermi levels are calculated to be located about 12 meV above the conduction band edge (E_c). For device characteristics studies, in order to achieve a better comparison among the different materials, we follow Liu *et al.*[3] to adjust the source Fermi level (by slightly tuning the doping concentration) in order to keep a fixed OFF state current of 1 nA. The ON and OFF state conduction band profile of the device is shown in Fig. 3(c). It clearly shows the bend bending involved in switching the device from the OFF state to the ON state by a sufficient applied gate bias. The simulated channel conductance is shown against a varying gate bias for a 2.5 nm diameter MoS_2 SWNT MOSFET, in Fig. 3(d). Clearly, the channel conductance G_{CH} is quantized in units of $G_0 (= 4q^2/h)$, as is the case with CNT FETs.[23,25] We consider only two propagating modes per subband. The value of channel conductance for ON condition ($V_D = 0.6$ V and $V_G = 0.4$ V) is evaluated to be $0.786\,G_0$. It was also observed that for low voltage operation, the channel conductance increased almost linearly with voltage. This is consistent with the findings of other groups for coaxial gate CNT FET.[23,25] Fig. 3(e) shows the transmission spectra for a 2.5 nm MoS_2 SWNT device in equilibrium condition ($V_D = V_G = 0$) and the non-equilibrium condition ($V_D = 0.6$, $V_G = 0$). Under the influence of a positive applied bias, the amplitude corresponding to the HOMO levels is suppressed. The transmission peak is centered at the LUMO levels in the non-equilibrium condition. For our NEGF studies, we consider the energy range of -1.75 to $+1.75$ eV, which includes the transmission peak at around E = 1.04 eV.

Figs. 4(a)–4(e) show the simulated output characteristics of the MX_2 nanotube surround gate MOSFETs. From the results (Figs. 4(a) and 4(b)), we observe the WS_2 and the WSe_2 tubes offer a higher ON current compared to the MoS_2 and the $MoSe_2$ nanotube FETs. The ON/OFF ratio of the SG-MOSFETs is calculated to be $\sim 0.6 \times 10^5$–0.8×10^5. The value of the subthreshold slope comes out as ~62.22 mV/decade. The drain induced barrier lowering (DIBL) is greatly suppressed in such MOSFETs and it is calculated to be only 12–15 mV/V. The simulated transconductance is shown in Fig. 4(c). The peak transconductance occurs at a gate voltage of 0.26 V, and its value is in the range 175–218 μS, with WSe_2 showing the highest g_m and MoS_2 the least.

The g_m/I_D ratio which is an important parameter for analog circuit design, is shown in Fig. 4(d). It is in the range 13.92–13.97 V^{-1} and remains fairly constant up to drain currents of 0.3 μA. There is not much variation in this parameter with the change of nanotube material.

The cut-off frequencies of the MOSFETs are calculated as $f_T \approx (g_m/2\pi C_G)$, where C_G is the gate capacitance of the co-axial gate.[25] The simulated f_T in Fig. 4(e) show a

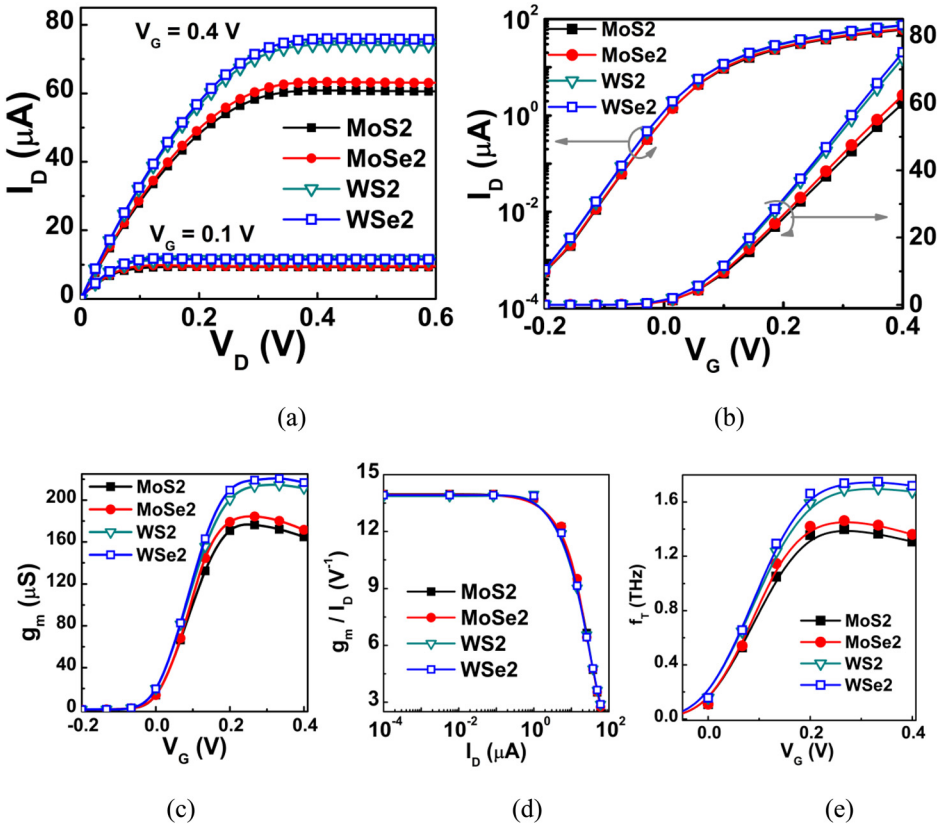

FIG. 4. (a) The simulated I_D-V_D characteristics and the (b) I_D-V_G characteristics ($V_D = 0.4$ V) of the MX_2 nanotube surround gate MOSFETs. (c) Simulated transconductance (g_m) for varying gate voltage (d) Simulated g_m/I_D ratio and (e) calculated cut-off frequencies for MX_2 SWNT MOSFETs.

maximum cut-off frequency of 1.395 THz for MoS_2 nanotube FET and 1.737 THz for the WSe_2 nanotube FET, with those for the WS_2 and the $MoSe_2$ are 1.45 THz and 1.68 THz, respectively.

Our simulated results for ON currents are in the range of 61–76 μA for 4.5 nm diameter tubes. We compare this with International Technology Roadmap for Semiconductors (ITRS) recommended values of drive currents per unit width for planar MOSFET by considering a planar MOSFET with channel width equal to the circumference of the nanotube (Fig. 5). We find that MX_2 SWNT surround gate MOSFETs provide sufficient ON currents as per ITRS requirements for

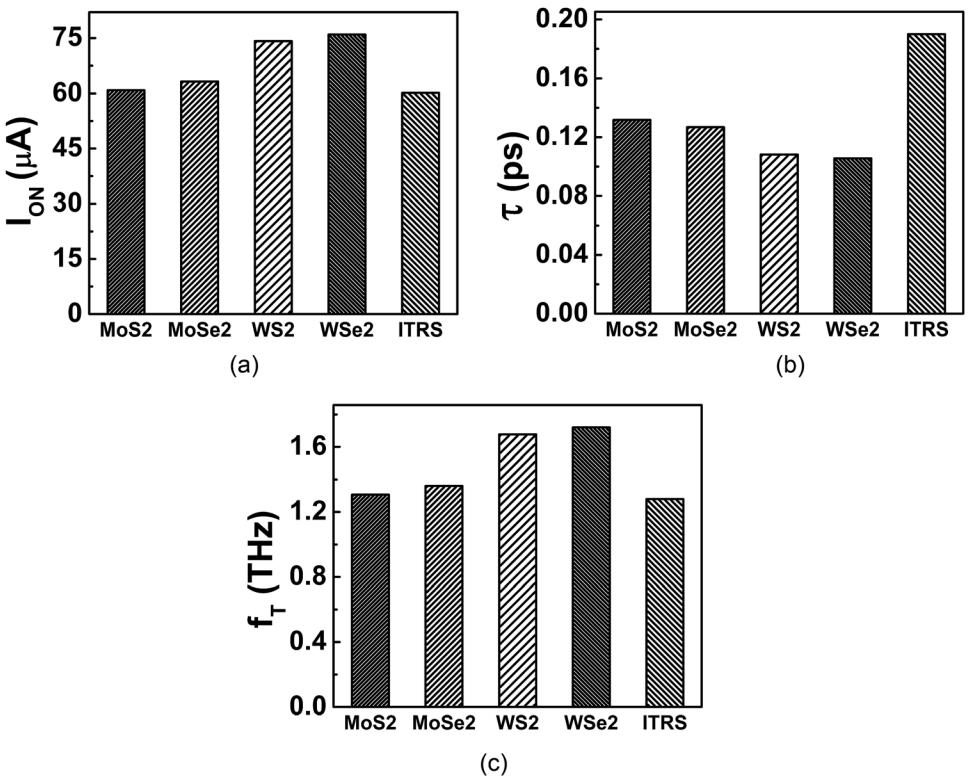

FIG. 5. Comparison of simulated output parameters of various MX_2 SWNT MOSFETs with ITRS recommendations for equivalent 10 nm planar technology node.

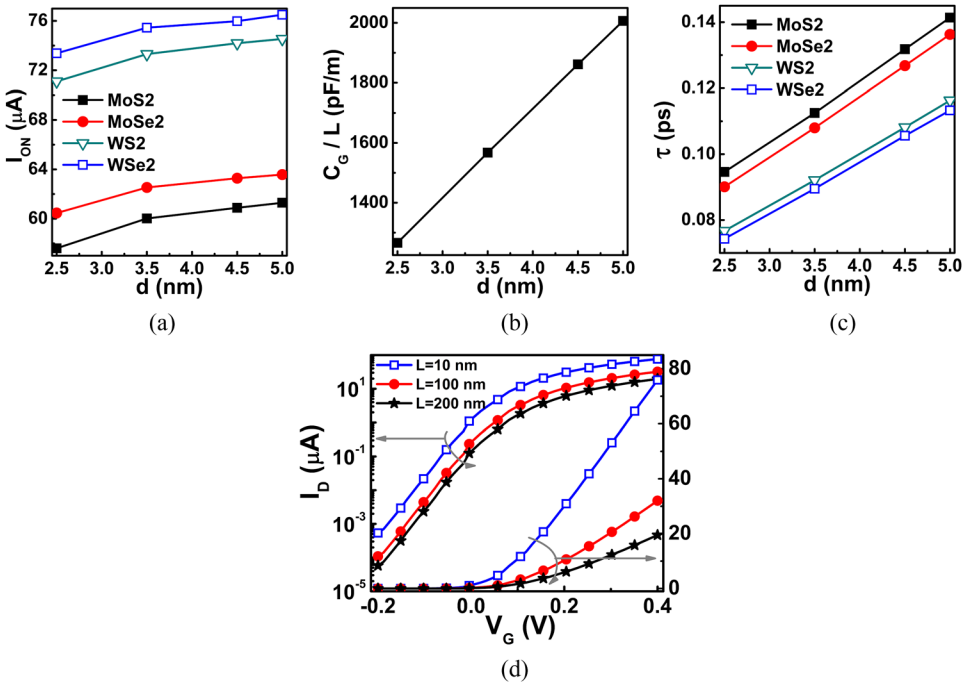

FIG. 6. Variation of (a) simulated ON currents, (b) gate capacitance per unit channel length, and (c) intrinsic delay time for varying SWNT diameter. (d) I_D-V_G output characteristics ($V_D = 0.4$ V) for WSe_2 SWNT surround gate MOSFETs for short (10 nm) and long (100, 200 nm) channel lengths, long channel values obtained by projected backscattering method.

10 nm high performance (HP) logic nodes.[34] Also, the value of intrinsic delay time shown in Fig. 5(b) (calculated as $\tau = C_G V_{dd}/I_{ON}$, where V_{dd} is the power supply voltage which as per ITRS recommendations for 10 nm HP node is taken to be 0.7 V and I_{ON} the ON current) is well within ITRS recommendations.[26] The simulated values of cut-off frequencies in Fig. 5(c) show good applicability of such MX_2 nanotube FETs for RF applications as per the ITRS recommendations for RF and Mixed Signal CMOS for 10 nm technology node.[35]

The results presented so far are all based on a device with 4.5 nm SWNT diameter and channel length of 10 nm. Though most MX_2 nanotubes experimentally reported have diameters in this 4–5 nm range, we look to further study SWNT of smaller diameters of 2.5 and 3.5 nm for their MOSFET applications. For this purposes, we use the calculated effective masses of SWNTs of varying diameter as already shown in Fig. 3(b) and use it in our NEGF simulations. The oxide thickness and other dimensions are considered to remain constant.

We observe in Fig. 6(a) that with decrease in SWNT diameter, there exists a slight decrease in the ON currents and a considerable decrease in the intrinsic delay time. For a reduction of nanotube diameter from 5 nm to 2.5 nm, the ON current for the WSe_2 device drops by ~4% and that for the MoS_2 device by ~6.5%. For the intrinsic delay time (τ), shown in Fig. 6(c), there is a 33% reduction for MoS_2 and a 34.5% reduction for WSe_2 nanotubes upon the reduction of diameter from 5 nm to 2.5 nm. This reduction in delay time is mostly due to the ~36.9% decrease in the gate capacitance (Fig. 6(b)) as the inner radii of the co-axial HfO_2 gate dielectric of thickness 2.5 nm decreases due to smaller SWNT diameter. Hence despite a ~4%–6% fall in the ON current, the delay time is reduced significantly.

As most of the experimentally fabricated nanotubes of MX_2 have lengths of few hundred nanometers to few microns, we also study the impact of having such long channel lengths on surround gate SWNT MOSFETs. For this purpose, we consider a projected current method that incorporates the effect of scattering in such long channels, as described in Sec. II. We take the WSe_2 nanotube surround gate MOSFET of 100 nm and 200 nm channel lengths, for studying the effect of channel length (L) on output characteristics. In Fig. 6(c), we see that for $L = 100$ nm, there is a 62.5% decrease in the drive current compared to the ballistic transport in short ($L = 10$ nm) channel devices. For 200 nm channel, this reduction is 75%. For the subthreshold slope (SS), it is calculated that for $L = 100$ nm, the value of SS is about 60.13 mV/decade and for $L = 200$ nm it is ~60.05 mV/decade, which is slightly less than that for 10 nm channel (SS ~ 62.22 mV/decade).

IV. CONCLUSION

We theoretically analyze the performance of MoS_2, $MoSe_2$, WS_2, and WSe_2 single wall armchair (n,n) nanotube surround gate MOSFET, in the 10 nm technology node. The material properties of the nanotubes are evaluated from DFT studies. The ballistic device characteristics are obtained by self-consistent the Poisson-Schrödinger solutions performed under the NEGF formalism. The MX_2 nanotube FETs show sufficiently good performance in terms of ON currents, ON/OFF ratio, transconductance, intrinsic delay time, and cut-off frequencies, for their possible applications in the 10 nm technology node. Among the materials studied, the tungsten dichalcogenide nanotubes offer superior device output characteristics compared to the molybdenum chalcogenide nanotubes, with WSe_2 showing the best performance. Studying SWNT diameters of 2.5–5 nm, it is found that increase in diameter provides smaller carrier effective mass and higher ON currents. Using mean free path calculation to project the quasi-ballistic currents, reduction in drain current

in long channel lengths of 100, 200 nm is also evaluated. The various simulation results show good promise for application of MX_2 SWNT surround gate ballistic MOSFETs for high performance logic and RF/mixed signal operations in the 10 nm technology node.

ACKNOWLEDGMENTS

A.S. acknowledges the Department of Science and Technology, Government of India for his DST Post-doctoral Fellowship in Nano Science and Technology. This work was supported by the Department of Science and Technology, Government of India under Grant No. SR/S3/EECE/0151/2012.

[1]B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, Nature Nanotechnol. **6**, 147 (2011).
[2]B. Radisavljevic, M. B. Whitwick, and A. Kis, ACS Nano **5**, 9934 (2011).
[3]L. Liu, S. B. Kumar, Y. Ouyang, and J. Guo, IEEE Trans. Electron Devices **58**, 3042 (2011).
[4]Y. Yoon, K. Ganapathi, and S. Salahuddin, Nano Lett. **11**, 3768 (2011).
[5]K. Alam, R. K. Lake, and S. Member, IEEE Trans. Electron Devices **59**, 3250 (2012).
[6]J. Zang, S. Ryu, N. Pugno, Q. Wang, Q. Tu, and M. J. Buehler, Nature Mater. **12**, 321 (2013).
[7]H. Tao, K. Yanagisawa, C. Zhang, T. Ueda, A. Onda, N. Li, T. Shou, S. Kamiya, and J. Tao, Cryst. Eng. Comm. **14**, 3027 (2012).
[8]O. Hod, J. Peralta, and G. Scuseria, Phys. Rev. B **76**, 233401 (2007).
[9]L. Margulis, P. Dluzewski, Y. Feldman, and R. Tenne, J. Microscopy **181**, 68 (1996).
[10]A. Rothschild, S. R. Cohen, and R. Tenne, Appl. Phys. Lett. **75**, 4025 (1999).
[11]M. Nath and C. N. R. Rao, Chem. Commun. 2236 (2001).
[12]S. M. Dubois, A. Lopez-bezanilla, A. Cresti, Ḱ. Franc, B. Biel, J. Charlier, and S. Roche, ACS Nano **4**, 1971 (2010).
[13]H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, Nano Lett. **12**, 3788 (2012).
[14]H. Iwai, Microelectron. Eng. **86**, 1520 (2009).
[15]K. J. Kuhn, M. Y. Liu, and H. Kennel, in *Proceedings of International Workshop on Junction Technology (IWJT)* (2010), p. 1.
[16]G. Seifert, H. Terrones, M. Terrones, G. Jungnickel, and T. Frauenheim, Phys. Rev. Lett. **85**, 146 (2000).
[17]E. W. Bucholz and S. B. Sinnott, J. Appl. Phys. **112**, 123510 (2012).
[18]P. Lu, X. Wu, W. Guo, and X. C. Zeng, Phys. Chem. Chem. Phys. **14**, 13035 (2012).
[19]See http://www.quantumwise.com/ for QuantumWise Atomistix ToolKit (ATK).
[20]W. Kohn and L. J. Sham, Phys. Rev. **140**, A1133 (1965).
[21]H. J. Monkhorst and J. D. Pack, Phys. Rev. B. **13**, 5188 (1976).
[22]See http://fysik.dtu.dk/ase/ase/optimize for ASE code in BFGS optimization method.
[23]J. Guo, M. Lundstrom, and S. Datta, Appl. Phys. Lett. **80**, 3192 (2002).
[24]S. Datta, *Quantum Transport: Atom to Transistor*, (Cambridge University Press, NY 2005).
[25]J. Guo, S. Datta, M. Lundstrom, and M. P. Anantram, "Towards Multiscale Modeling of Carbon Nanotube Transistors," International J. on Multiscale Computational Engineering, special issue on multiscale methods for emerging technologies, ed. N. Aluru, **2**, 257–276 (2004).
[26]Z. Ren, "Nanoscale MOSFETS: Physics, design and simulation," Ph.D. dissertation (Purdue University, 2001).
[27]I. Milošević, B. Nikolić, E. Dobardžić, and M. Damnjanović, Phys. Rev. B **76**, 233414 (2007).
[28]G. L. Frey, S. Elani, M. Homyonfer, Y. Feldman, and R. Tenne, Phys. Rev. B **57**, 6666 (1998).
[29]G. L. Frey, R. Tenne, M. J. Matthews, M. S. Dresselhaus, and G. Dresselhaus, J. Mater. Res. **13**, 2412 (1998).
[30]*Nanotube and Nanofibers*, edited by Y. Gogotsi (CRC Press, Boca Raton, 2006) Vol. 978, pp. 144.
[31]M. Cote, M. L. Cohen, and D. J. Chadi, Phys. Rev. B **58**(8), R4277 (1998).
[32]Q.-C. Sun, L. Yadgarov, R. Rosentsveig, G. Seifert, R. Tenne, and J. L. Musfeldt, ACS Nano **7**, 3506–3511 (2013).
[33]L. Yadgarov, R. Rosentsveig, G. Leitus, A. Albu-Yaron, A. Moshkovich, V. Perfilyev, R. Vasic, A. I. Frenkel, A. N. Enyashin, G. Seifert, L. Rapoport, and R. Tenne, Angew. Chem., Int. Ed. Engl. **51**, 1148 (2012).
[34]International Technology Roadmap for Semiconductors, 2011 PIDS Report, http://www.itrs.net/Links/2011ITRS/Home2011.htm.
[35]International Technology Roadmap for Semiconductors, 2011 RFAMS Report, http://www.itrs.net/Links/2011ITRS/Home2011.htm.