Demonstration of intrinsic STDP learning capability in all-2D multi-state MoS_2 memory and its application in modelling neuromorphic speech recognition

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The human brain can be characterized by its large number of adaptive synapses, connecting billions of neurons capable of both learning and perceiving the environment. Neuromorphic computing, based on brain-inspired principles, is a promising technology, to build low-power, distributed, fault-tolerant intelligent systems mainly for perception tasks. Here, we demonstrate the intrinsic capability of floating gate (FG) MoS_2 device (MoS_2 FG-FET) to model the spike time dependent plasticity (STDP) learning rule that is based on the transient response of the MoS_2 channel to spikes applied to the source and gate leads. We implemented the STDP learning protocol in a neuromorphic speech recognition system (NSRS), inspired by the human auditory pathway, for various auditory recognition tasks. Our proposed NSRS consists of a cochlea model, an unsupervised feature learning stage and a simple linear classifier. The unsupervised learning stage uses the biologically plausible STDP learning in novel two-dimensional MoS_2 FG-FET memory which circumvents the requirement of any other learning circuitry.

Keywords: Neuromorphic computing, electronic cochlea, brain-inspired learning, emerging devices, beyond CMOS, MoS_2 memristors

I. INTRODUCTION

von-Neumann architecture, introduced by John von Neumann in 1945, is the most widely used architecture in modern computing devices[1]. A key feature of this framework is the utilization of dedicated hardware components for computation and storage. Improvements in fabrication capabilities have resulted in an increase in the number of transistors per microchip, augmenting both the speed of computation and storage space available. However, this architectural framework wih a separation between the computation and storage units makes it inefficient at solving problems that require simultaneous processing of large amounts of data. These mostly include ill-defined constructs such as image, speech or pattern recognition and necessiate a learning capability similar to that in a biological brain. Meeting the computational challenges posed by problems of an ill-defined nature necessiates an architecture capable of in-memory computing, analogous to the synapses in a brain[2]. Silicon-based synapses with learning capabilities like spike time dependent plasticity (STDP) (the variation of synaptic conductance with time difference (Δt) between pre- and post-synaptic spikes) have been demonstrated[3–5]. However, integration complexities due to short-channel effects and high switching power in devices based on silicon nanotechnology, makes it fundamentally difficult to attain the synaptic density (~ 10^{10} synapses per cm^2 as in the human brain) and energy efficiency necessary for neuromorphic computing.

Investigating an alternative hardware platform based on two-dimensional (2D) materials has certain advantages over silicon[6]. The atomic confinement leads to strong gate coupling, suppresses short-channel effects and reduces device footprints[7–9] which is ideal for large neuromorphic systems. Furthermore, advancement of fabrication techniques allows for the vertical and lateral stacking of different 2D materials into heterostructures with clean interfaces. This introduces flexibility in device design resulting in unique device architectures for electronics[10–14], optoelectronics[15–18]and memory applications[12,19–22] with functionalities often surpassing those of silicon-based solutions. MoS_2 is of particular interest in this context because of its large intrinsic band gap[23], high ON/OFF ratio[12,21], near-ideal subthreshold swing[21,24] and high carrier mobility[25]. These properties make MoS_2 an ideal candidate for low-power in-memory computing applications for edge devices[26–28].

Several architectures for 2D memory have already been explored. These include, intercalation of ions using liquid gates in MoO_3[29] and WSe_2[30], filament formation in MoS_2[31] and defect induced resistive switching in *h*-BN[32,33]. However, these methods either use ionic liquids which are environment sensitive and degrade with time or are dependent on the defect densities in the nanosheets which are difficult to control. There have also been reports of 2D materials with STDP capabilities using copper filament formation in MOCVD grown MoS_2 flakes[31]. Although the vertical geometry reduces device footprint,

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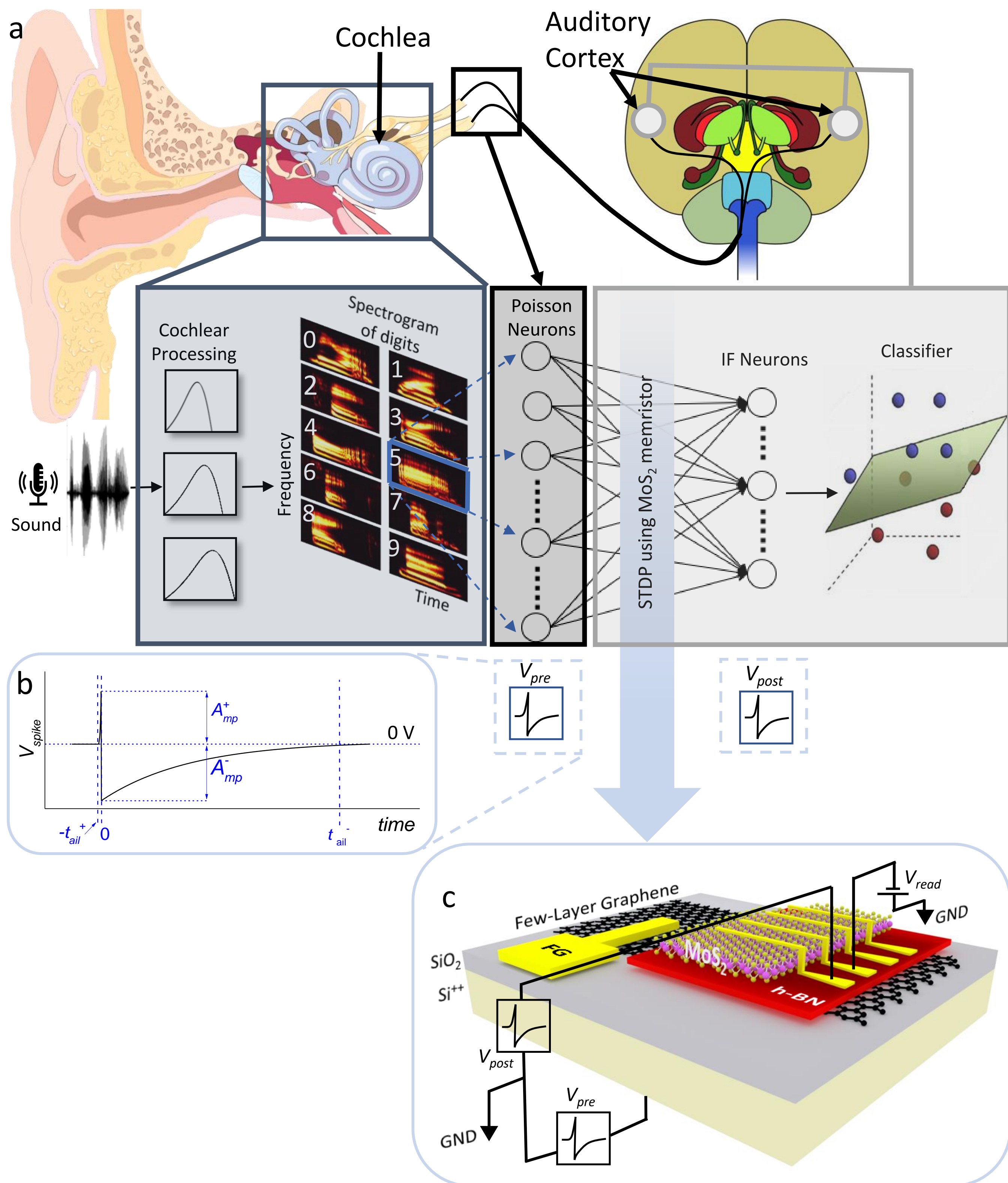

FIG. 1: **Neuromorphic speech recognition system (NSRS)**. **a**, Block diagram of the proposed NSRS compared with its biological counterpart. The cochlear processing unit filters various frequency components from the raw audio samples and performs nonlinear transduction, to mimic basilar membrane (BM) and inner hair cells (IHC) functions respectively. Output spectrogram of digits 0-9 is shown. Poisson neurons model the spiral ganglion cell (SGC) and features are extracted through the STDP Layer to the output neurons. The postsynaptic potential at the output neurons are used to perform speech recognition task on TIDIGITS isolated digits. **b**, Typical shape of a bio-realistic spike used in the STDP layer. **c**, Schematic of the MoS_2 FG-FET used for STDP learning. Details related to the MoS_2 FG-FET and $bio-realistic$ spike are presented in the main text.

the presence of copper filaments in both the low (LRS) and high (HRS) resistance states leads to a low ON/OFF ratio and reduces the range of accessible conductance states. In this work, we employ an all-2D architecture with a floating gate MoS_2 device from multilayer van der Waals heterostructure, where the operation of the device is entirely based on tunneling of charge across the layers. While 2D material-based FG memory has been demonstrated before, their usage was restricted to that of passive memristors describing analog memory behaviour[19,21,22,26,34–36]. **Notably, Kim *et al.*[37] demonstrated STDP in a FG carbon nanotube transistor. The authors achieve this by utilizing a 3T-Synapse, with the FG transistor acting as an analog memory. The current work demonstrates the inherent STDP learning capabilities in a single solid-state MoS_2 FG transistor without any additional circutit overheads.** The introduction of inherent learning capabilities like STDP, reduces hardware complexity by avoiding additional learning circuitry and is an important step towards developing emergent device platforms for neuromorphic applications.

We have considered the neuromorphic speech recognition system (NSRS), shown in Fig. 1a, to illustrate the utility of intrinsic STDP response in MoS_2 FG devices. The NSRS is inspired by the human auditory pathway, which represents a neuro-physical action where the cochlea transforms the incoming acoustic signal to a time-frequency map, also called a spectogram (schematic of the process is in Fig. 1a). The cochlea is a fluid-filled, spiral structure that transduces the mechanical vibrations received into waves, which vibrate the basilar membrane (BM). The movement of the BM varies at different locations within the cochlea, since the stiffness of the membrane gradually decreases from its basal end to the apex. Inner Hair Cells (IHCs) are the transducers, that help to convert the sound generated motion of the cochlea, to neurotransmitter release at synapses which excite the primary auditory neurons. After the cochlea, the second major transformation occurs at primary auditory cortex, where more complex processing takes place, such as high-level feature extraction followed by accoustic tasks such as speaker recognition, sound segregation, denoising, voice activity detection. This high-level feature extraction stage involves the learning of synaptic connections between the neurons in the cortical areas. The synaptic plasticity is the ability to strengthen or weaken synapses, based on the order of occurrence of the pre- and post-synaptic neuronal spikes. The synapses are increased in strength if presynaptic spikes repeatedly occur before postsynaptic spikes, within a range of few milliseconds, otherwise they are decreased in strength for the opposite temporal order[38].

The NSRS depicted in Fig. 1a can be broadly divided into three blocks. The first stage, or the cochlea, converts the sound waves into neural spikes that act as inputs for the feature learning stage. The second stage comprises of a neural network. An important aspect of this stage is the inherent plasticity of the synaptic transistors which is used to model the STDP learning rule. We demonstrate here that individual MoS_2 FG-FET is capable of exhibiting such STDP learning capability, that will allow for unsupervised feature learning within the MoS_2 FG-FET without the necessity of additional learning circuitry. In the final stage, the classification performance of the system is checked for a target application using a linear classifier. The key advantage of realizing STDP capability on an all-2D MoS_2 FG-FET is that it is based entirely on the gate-controlled charge transfer across different layers of a van der Waals heterostructure, and thus highly tunable both in response time and magnitude. This reflects in the maximum conductance change ($\Delta G\%$) observable in STDP behaviour to be $\geq 100\%$ for MoS_2 FG device (Fig. 3e and Fig. 6a). **Larger changes in conductance allow for distinct, separated states and improve the temporal sensitivity of the STDP response[39]. The number of states attainable in a multi-state memory device is governed by two factors, the range of accessible conductance values and the temporal stability of each state. The former provides a choice of conductance values for possible memory levels while the latter defines how closely spaced these levels can be. Apart from quantum confined states such as those observed in the quantum hall effect[40], memory levels are not perfectly stable and are prone to conductance decay, which occur, for example, in FG memory devices, due to dielectric relaxation, leakage of carriers through defects in the dielectric, thermal excitation etc.[41]. A larger operation range in conductance facilitates a larger choice of states which corresponds to a larger choice of time difference Δt between the pre- and post-synaptic spikes for the STDP response. This makes it possible to have distinct states which are separated by small differences in Δt and hence, a better temporal sensitivity. The methodology used for determining the number of states in the current work is presented in Section II C.**

The manuscript is organized as follows. In Section II A, we describe the electrical characterization and STDP response in MoS_2 FG-FET. Section II B outlines the performance of the NSRS trained using the inherent STDP of the MoS_2 synapse and Section II C investigates the effects of device-to-device mismatch on the performance of the NSRS. We conclude with a brief discussion of the main observations and future possibilities.

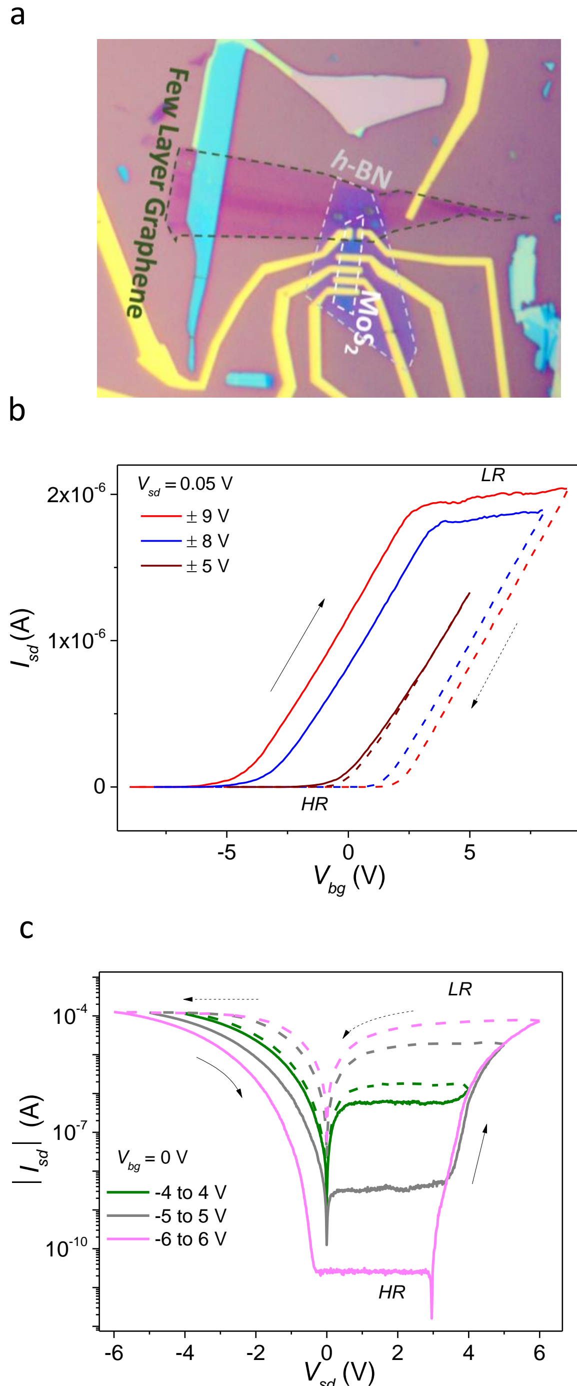

FIG. 2: **Electrical characterization of MoS_2 FG-FET.** **a**, Optical micrograph of a typical MoS_2 FG-FET with individual layers outlined. **b**, and **c**, show the transfer and output characteristics, respectively, for MoS_2 FG-FET. Solid lines denote forward sweep directions (from -ve to +ve values) and dashed lines reverse sweep directions (from +ve to -ve values) in both graphs.

II. EXPERIMENTAL RESULTS

A. STDP in the MoS_2 FG-FET

Fig. 2a shows the optical micrograph of a typical MoS_2 synaptic device with dashed lines outlining the component atomic layers. The device geometry consists of a top MoS_2 layer, the channel, and bottom few layer graphene (FLG) FG, which are separated by a *h*-BN tunnel barrier. The complete stack is placed on an Si^{++}/SiO_2 (285 nm) substrate acting as the back-gate (Fig. 1c). We fabricated the device using a dry stacking technique to assure clean interfaces for better performance. Details related to the fabrication technique are provided in the Methods Section (Section IV). **We demonstrate the transfer and output characteristics of typical MoS_2 FG-FET devices in Fig. 2b and c, respectively. The transfer characteristics (Fig. 2b) are obtained by sweeping the back gate voltage (V_{bg}) while maintaining a constant source-drain bias (V_{sd}) of 0.05 V. The output characteristics (Fig. 2c) are measured by varying the V_{sd} at a constant V_{bg} = 0 V.** All MoS_2 FG-FET devices studied in this work demonstrate a large hysteresis in both the transfer (Fig. 2b) and output characteristics (Fig. 2c) with distinct low resistance (LR) erase and high resistance (HR) program states. The hysteresis is known to originate from field assisted tunneling and subsequent trapping of charges in the FG due to the applied gate or drain bias[21]. A temporal control over the charge tunneling leads to analog memory behaviour as outlined in Ref. [21] and Supplementary Section [III]. The resulting conductance states are a pre-requisite for demonstrating learning mechanisms like STDP. **The devices also demonstrate near ideal subthreshold swing of ~85 mV/decade for over three decades of current and large ON/OFF ratios of ~ 5×10^5 (Supplementary Section VII).**

Our previous work[21] demonstrated the synaptic properties like pulsed potentiation and depression, and paired pulse potentiation (PPF) using the current device geometry. However, the demonstration of STDP used a combination of multiplexer and the FG device, resulting in additional circuit overhead as well as increased complexity. **The current work rectifies these issues by demonstrating an intrinsic STDP learning rule in MoS_2 FG-FET using the method of overlapping pulses[39,42].** As previously reported[42], the shape of the spike plays a very important role in determining the nature of STDP response. The MoS_2 FG-FETs demonstrate STDP response for different pulse shapes (Supplementary Section [IV]), however, bio-realistic pulses with a functional form similar to action potentials in the nervous system[38] (Fig. 1b) result in STDP responses that

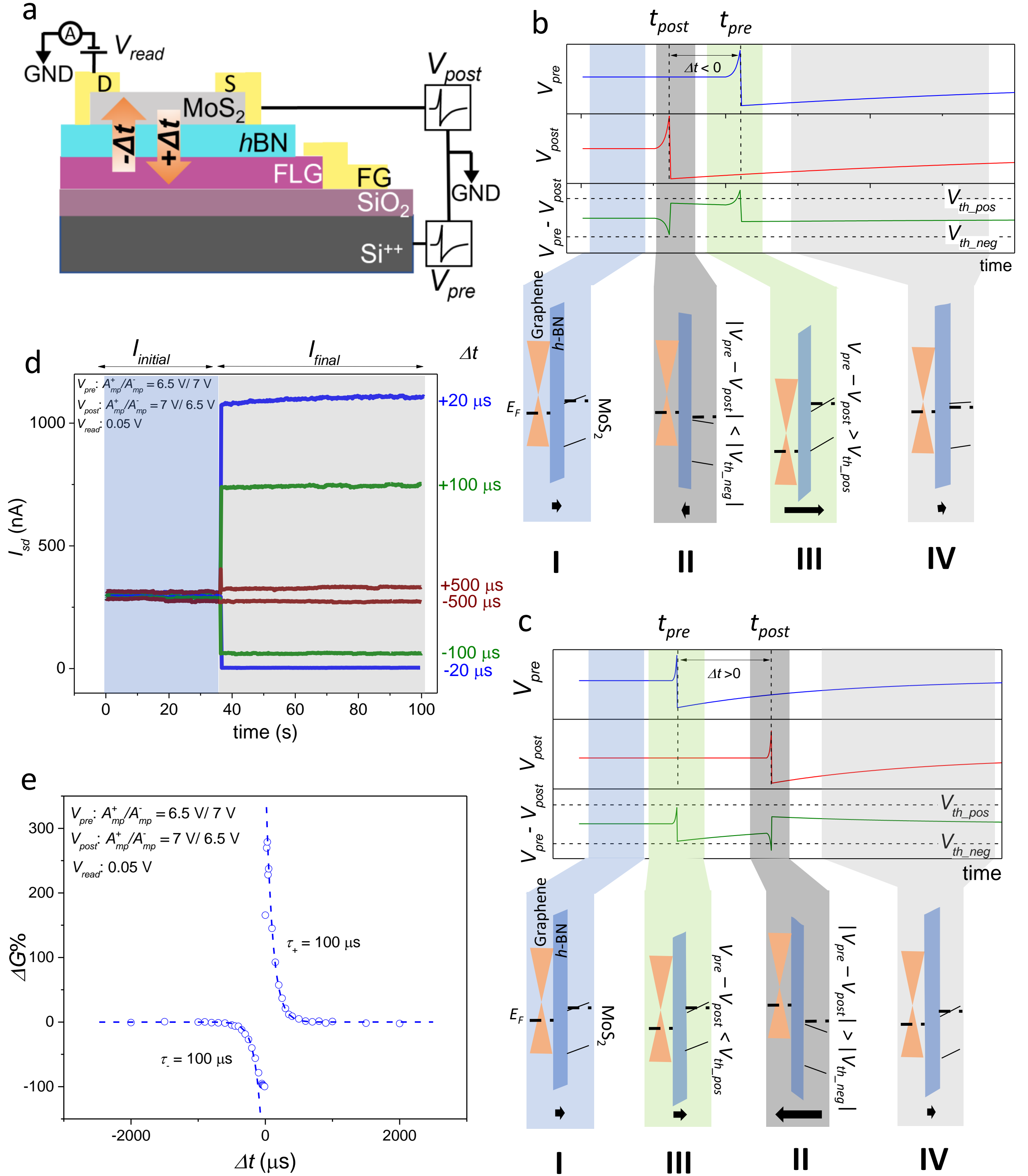

FIG. 3: **Spike time dependent plasticity (STDP) in MoS_2 FG-FET.a**, Circuit configuration for STDP measurements. Gate and source are considered as the pre- and post-synaptic terminals, respectively. The arrows show the direction of tunnel current (I_{tunnel}) for positive and negative Δt. Top and middle horizontal panels of **b**, and **c**, depict the pre- and post-synaptic spikes for a $-ve$ and $+ve$ Δt, respectively. The bottom panel shows the resulting overlap potential ($V_{pre} - V_{post}$). Vertical panels (I-IV) at the bottom of the figures demonstrate the band configuration for four different regimes of the overlap potential. Magnitude and direction of the tunneling current I_{tunnel} are indicated by the size and direction of black arrow at the base of each panel, respectively. **d**, Temporal response of the MoS_2 FG-FET to a pair of pre- and post-synaptic spikes. $I_{initial}$ and I_{final} represent the channel current before and after the application of the spikes, respectively, for a V_{read} = 0.05 V. **e**, Graph showing the variation of $\Delta G\%$ as a function of Δt. The experimental data is indicated by open circles while the dashed line is an exponential fit following Eq. 2.

are comparable to biological systems and is the pulse shape of choice for this work.

Fig. 1b shows a typical spike which can be modelled in the following fashion. **The spike onset is marked by the time-period t^{+}_{ail} (= 10 μs) when an exponential rise to the positive peak amplitude of A^{+}_{mp} from the rest potential (0 V) commences with a small time constant ($\zeta^{+} = 3\ \mu$s).** This is followed by a sharp decrease in the voltage to the negative peak amplitude of -A^{-}_{mp} at which time a slow exponential decay with large time constant (ζ^{-} = 330 μs) takes the spike voltage to its resting value over a time period t^{-}_{ail} (= 1 ms). The functional dependence of V_{spike} is given by[42]

$$V_{spike}(t) = \begin{cases} A^{+}_{mp}\dfrac{e^{\frac{t}{\zeta^{+}}} - e^{\frac{-t^{+}_{ail}}{\zeta^{+}}}}{1 - e^{\frac{-t^{+}_{ail}}{\zeta^{+}}}}, & if\ \ -t^{+}_{ail} < t < 0 \\ -A^{-}_{mp}\dfrac{e^{\frac{-t}{\zeta^{-}}} - e^{\frac{-t^{-}_{ail}}{\zeta^{-}}}}{1 - e^{\frac{-t^{-}_{ail}}{\zeta^{-}}}}, & if\ \ 0 < t < t^{-}_{ail} \end{cases} \quad (1)$$

To measure the STDP response, spikes are applied to the pre- (V_{pre}) and post- (V_{post}) synaptic terminal (source and gate, respectively) of the MoS_2 FG-FET (Fig. 3a) with a pre-defined time difference ($\Delta t = t_{post} - t_{pre}$) as depicted in Fig. 3b, c. A small read voltage (V_{read} = 0.05 V) is also applied to measure the changes in channel current, which reflects the change in conductance (Details in the Methods Section (Section IV)). Fig. 3d shows the time series response of a typical MoS_2 FG-FET to pre- and post-synaptic spike pairs with different Δt values. **I_{inital} and I_{final} represent the channel current before and after the application of the pre- and post-synaptic spikes. The measurements are performed by applying pre- and post-synaptic spikes with A^{+}_{mp}/A^{-}_{mp} values 6.5 V/7 V and 7 V/6.5 V, respectively.** The channel conductance increases (decreases) for positive (negative) Δt values with larger changes for smaller time differences, mimicking the observations in biological synapses following STDP protocol[38]. The STDP behaviour is also demonstrated by plotting the percentage change in device conductance $\Delta G\ \% = (I_{final} - I_{inital})/I_{initial}$ (computed from the time series data shown in Fig. 3d) as a function of Δt which is depicted in Fig. 3e for a starting conductance of 6 μS. We observe an exponential reduction in ΔG% with increasing Δt which is modelled as follows

$$\Delta G\% \propto \begin{cases} e^{\frac{-\Delta t}{\tau_{+}}}, & if\ \ \Delta t \geq 0 \\ e^{\frac{+\Delta t}{\tau_{-}}}, & if\ \ \Delta t \leq 0 \end{cases} \quad (2)$$

where τ_{+} and τ_{-} denote the timescales for which the synaptic device remains sensitive to the pre- and post-synaptic spiking.

The microscopic origin of the plasticity of the device (Fig. 3e) can be explained from the time dependent overlap potential ($V_{pre} - V_{post}$) of the pre- and post-synaptic spikes (Fig. 3b and c). We observe that the tunneling of charges and consequent changes in synaptic weights are only possible when this voltage is above a threshold voltage. Negative values of Δt (Fig. 3b) result in an increase of the overlap potential above V_{th_pos} leading to a decrease in channel conductance while for positive Δt values (Fig. 3c) the opposite scenario occurs resulting in a decreased channel resistance. The positive (V_{th_pos}) and negative (V_{th_neg}) threshold voltages are indicated by dashed lines in the bottom panel of Fig. 3b and c.

The overlap potential can be broadly divided in four regions. Fig. 3b and c demonstrates this for a negative and positive Δt, respectively. Since both the scenarios can be explained by similar arguments, we limit ourself to the discussion of negative Δt values (Fig. 3b). Region I shows the band alignment before the arrival of pre- or post-synaptic spike with both pre- and post-synaptic potentials at their resting values. The MoS_2 channel has a finite conductance indicating some effective positive charge on the FG. However, the potential across the h−BN tunnel barrier is insufficient for the tunneling of charges leading to a negligible tunnel current (I_{tunnel}). This is indicated by the small arrow at the base of the panel. The size and direction of the arrow represents the magnitude and direction of I_{tunnel}, respectively. Region II denotes the arrival of the post-synaptic spike with the pre-synaptic spike at rest-value. The positive voltage on the source terminal reduces the potential of the MoS_2 channel relative to the FG, but since $V_{pre} - V_{post} < V_{th_neg}$, there is negligible I_{tunnel} and consequently no long term changes in channel conductance. Region III represents the arrival of the pre-synaptic spike while the post-synaptic potential is returning to its resting value. Now, $V_{pre} - V_{post} > V_{th_pos}$, leading to a considerable I_{tunnel}, and an accumulation of negative charges on the FG. The enhanced negative charge on the FG leads to a decrease in channel conductance (negative ΔG%) for negative Δt (Panel IV). We define V_{th_pos} (V_{th_neg}) as the maximum positive (negative) peak voltage of the overlap potential for the largest negative (positive) time difference Δt at which a $|\Delta G\%| > 3\%$ is observed. For the DUT, we find, $V_{th_neg} \approx -8$ V, and $V_{th_pos} \approx 7.6$ V.

For a quantitative analysis, we hypothesize[21] that the experimentally observed STDP behavior of the MoS_2 FG-FET, occurs due to an electric field (E_{tunnel}) driven tunneling of charges from the channel to the FG. In the context of our device geometry, E_{tunnel} is the electric field developed across the h-BN layer due to the voltage applied at the pre (gate) - and/or post (source) -synaptic terminal. This electric field results in a tunneling current (I_{tunnel}) which follows the Fowler Nordheim (FN) mechanism

$$I_{tunnel}(V) = \frac{A_{ch} q^3 m V^2_{tunnel}}{8\pi h \phi_b d^2 m^*} \exp[\frac{-8\pi\sqrt{2m^*}\phi_b^{\frac{3}{2}} d}{3hqV_{tunnel}}] \quad (3)$$

TABLE I: Range of tunnel barrier height for electrons and holes in MoS_2 FG-FET

Electron affinity of h-BN (eV) (χ^{h-BN})	**Band gap of h-BN (eV)** (λ^{h-BN})	**Work function of MoS_2 (eV)** (ϕ^{MoS})	**Electron barrier height (eV)** ($\phi_b^{electron} = \chi^{h-BN} - \phi^{MoS}$)	**Hole barrier height (eV)** ($\phi_b^{hole} = \chi^{h-BN} + \lambda^{h-BN} - \phi^{MoS}$)
1.1 - 2.3	5.2 - 5.9	4.6 - 4.9	2.6 - 3.5	1.7 - 3.3

where A_{ch} and d are the channel area and the thickness of the h-BN tunnel barrier, respectively, $V_{tunnel} = E_{tunnel} \times d$ is the tunnelling bias across the h-BN tunnel barrier and $m^* = 0.26m$ is the effective mass of charge carriers in h-BN[43]. The barrier height for tunnelling ϕ_b is the energy barrier at the MoS_2/h-BN junction and is calculated from the electron affinity of h-BN and work function of MoS_2 (Fig. 4a). From previous reports, the electron affinity and band gap of h-BN ranges between 1.1-2.3 eV[19,44] and 5.2-5.9 eV[19,44], respectively, while the work function of MoS_2 is 4.6-4.9 eV[19]. The corresponding range of ϕ_b values in the current device geometry is presented in the Table I.

The STDP response is numerically calculated by finding the $\Delta G\%$ for every Δt. To perform this, the overlap potential is discretized using a time interval of 0.1 μs. The tunnel bias V_{tunnel}, at each instant of time t_i, is given by the overlap potential modified by the potential of the FG (V_{FG}) at that instant of time.

$$V_{tunnel}(t_i) = V_{pre}(t_i) - V_{post}(t_i) + V_{FG}(t_i) \quad (4)$$

where, $V_{tunnel}(t_i)$, $V_{pre}(t_i)$, $V_{post}(t_i)$ and $V_{FG}(t_i)$ are the tunnel, pre-synaptic, post-synaptic and FG bias, respectively at the instant t_i. Here, we have assumed that the total applied bias (V_{pre}) is applied at the FG terminal. This is valid due to the capacitance engineering introduced by an extension of the FG[21]. For i=1, i.e. the first instant, $V_{FG}(t_1)$ is the gate bias above threshold needed to attain the initial conductance state of the device. This is demonstrated for an initial current of 300 nA and drain bias of 0.05 V in Fig. [4]b.

In response to the applied $V_{tunnel}(t_i)$, a tunnel current $I_{tunnel}(t_i)$ (Eq. 3) flows across the h-BN barrier leading to the storage of positive (negative) charges on the FG, thereby increasing (decreasing) its potential by

$$\Delta V_{FG}(t_i) = \frac{Q_{tunnel}(t_i)}{C_{self}} \quad (5)$$

where, $Q_{tunnel}(t_i) = I_{tunnel}(t_i) \times$ 0.1 μs, is the charge stored on the FG due to a single pulse and $C_{self} = 8\epsilon_0 A_{FG}$, is the self-capacitance of the FG with ϵ_0 the permittivity of free space and A_{FG} ($\approx$ 45000 μm^2) the area of the FG.

The FG potential is updated for the next instant (t_{i+1}) following

$$V_{FG}(t_{i+1}) = V_{FG}(t_i) + \Delta V_{FG}(t_i) \quad (6)$$

and the same is used to obtain the tunneling current for the next time interval using Eq. 3. Repeating this process for all t_i values gives us the total FG voltage change (ΔV_{FG_total}) for a pair of pre- and post-synaptic spikes separated by Δt.

$$\Delta V_{FG_total} = \sum_{i=1}^{N} \Delta V_{FG}(t_i) \quad (7)$$

ΔV_{FG_total} represents the total back-gate voltage change due to the overlapping of the pre- and post-synaptic spikes. The resulting change in the channel conductance is estimated from the transfer characteristics (Fig. [4]b) and the corresponding $\Delta G\%$ is computed.

The simulated plot, dashed line in Fig. 4c, is obtained by repeating the process for different Δt values and shows good agreement with the experimental data for hole and electron barrier of 2.66 eV and 3.04 eV, respectively. These values match closely with the reported values for MoS_2/h-BN interface presented in Table [I], making us believe that electric field dependent FN tunneling is at the heart of the observed STDP behaviour in MoS_2 FG-FET. A numerical analysis of the pulsed potentiation and depression behavior in the MoS_2 FG-FET devices and the energy dissipated during training and reading can be found in Supplementary Section [III] and [V] , respectively.

Notably, the STDP timescales (τ_+, τ_-) of ~100 μs obtained in Fig. 3e are smaller than the millisecond timescales observed in biological systems[38]. However, these timescales are tunable by changing the spike parameters. Fig. 4d demonstrates this for four different pre- and post-synaptic spike combinations. τ_+, τ_- and maximum $\Delta G\%$ increase with increasing spike amplitudes A^+_{mp} and A^-_{mp}. For a particular Δt, the magnitude of overlap potential ($V_{pre} - V_{post}$) and hence $\Delta G\%$ is determined by the magnitude of the pre and post-synaptic spike. Higher spike heights result in a larger overlap potential and tunnel current (Eq. 3). The increased storage of charges on the FG leads to greater changes in conductance lasting for a wider range of Δt values. We obtained a time-scale tunability over a factor of five by changing the pulsing amplitude, indicating a key advantage of pure electrostatic operation. This is an important feature and opens up the possibility of engineering tailor-made STDP responses for specific applications.

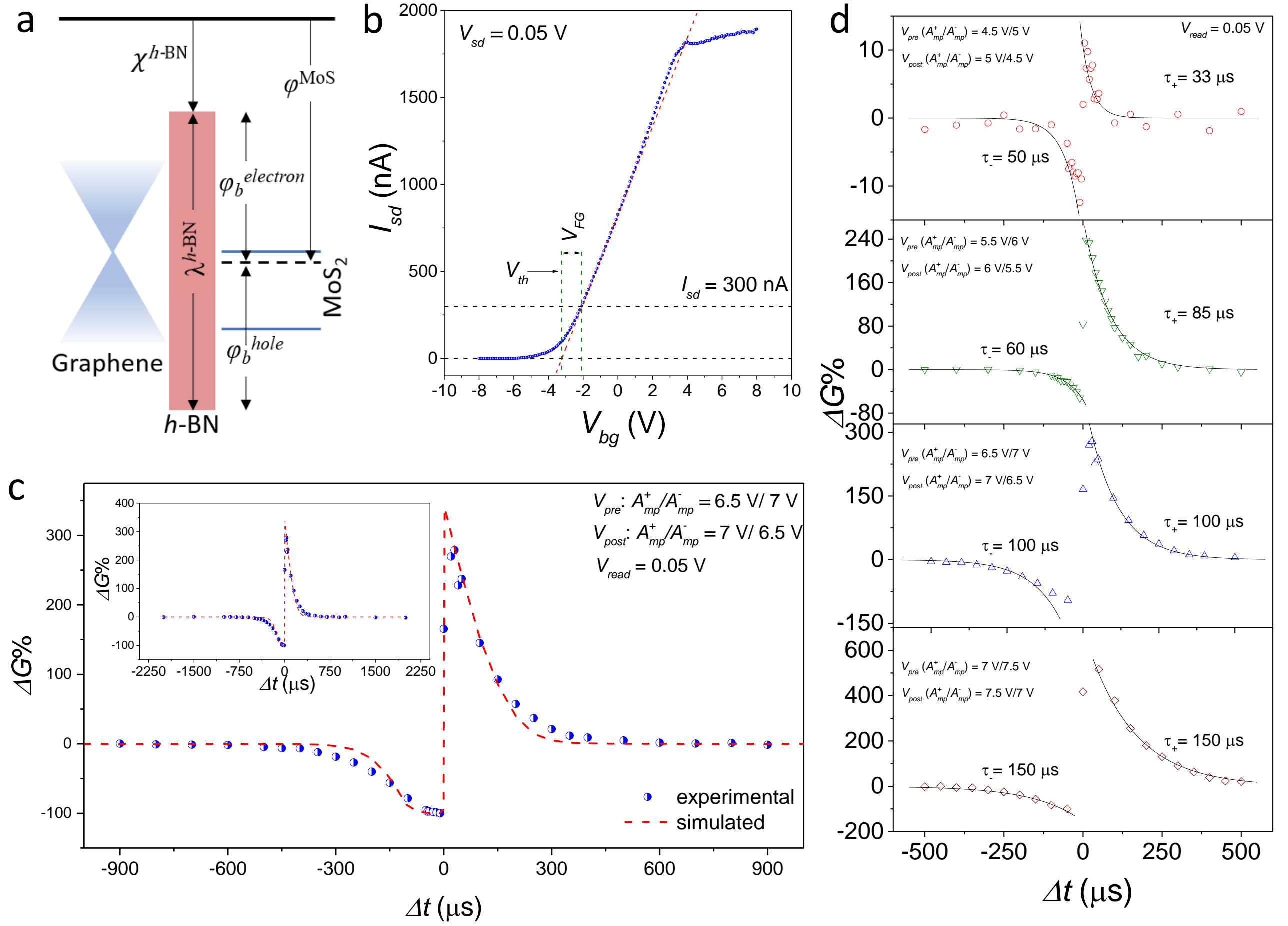

FIG. 4: **Modelling spike time dependent plasticity (STDP) in MoS_2 FG-FET**. **a**, Schematic depiction of the tunnel barrier height and band alignment at MoS_2/*h*-BN interface. **b**, Graphical determination of V_{FG} from the transfer characteristics. **c**, Experimentally observed (symbols) and numerically simulated (red dashed line) STDP characteristics of MoS_2 FG FET. Inset shows the full STDP response while the main panel zooms into time differences near $\Delta t = 0$ μs. **d**, From top to bottom panel. Graphs demonstrating STDP response for increasing spike heights. We find an increase in decay timescales for both positive (τ_+) and negative (τ_-) Δt with increasing spike height.

B. Cochlear recognition with STDP in MoS_2 FG-FETs

Our earlier work demonstrated the real-time hardware implementation[45] of a biologically plausible cochlea model known as Cascade of Asymmetric Resonators with Fast-Acting Compression (CAR-FAC) model[45,46]. The system proposed here only uses the CAR part of the model, which emulates the behavior of the BM, the IHC and the spiral ganglion cells (SGCs). The SGC is simply modelled as a Poisson process, which converts the IHC output into spike trains. The output of the IHC is the spectrogram , which is down sampled in time to reduce computational complexity (LHS of Fig. 5a). A detailed description of this block is provided in the Supplementary Section [I]. The spiked output of the SGCs are connected to the next layer with spiking neurons via adaptive synaptic connections, which learn acoustic features from the input using the STDP rule. The synapses in this unsupervised feature learning stage are implemented using a MoS_2 FG-FET acting as a multi-state memory with inherent STDP learning capability.

The update rule (mentioned in detail in Supplementary Section [II]) for all synapses connecting the pre- and post- synaptic neurons in the feature learning stage of the NSRS can be summarized using Eq. 2. For a relatively short ($\lesssim 0.5 \times \tau_{+/-}$) and long ($\gtrsim 4.5 \times \tau_{+/-}$) time interval, as compared to τ_+ and τ_-, synapses are not altered since they don't contribute to the post-synaptic firing. Otherwise, the synaptic weights, w, are updated with learning rate, η, times the conductance, $\Delta G\%$, corresponding to Δt. Since, the update rule is independent of the class of the spoken digit, the synapses of the output neurons in the neural network learns the auditory features using

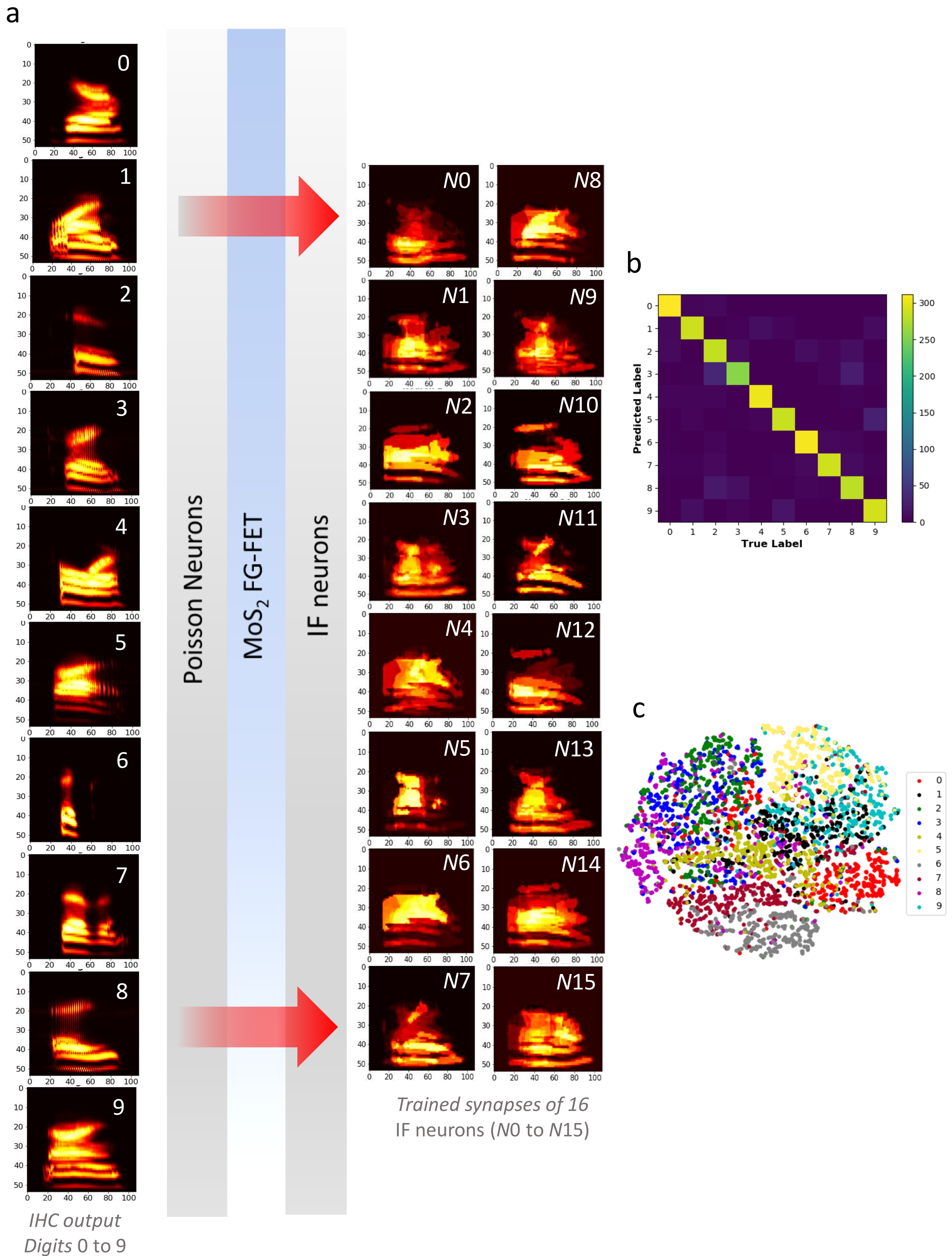

FIG. 5: **Speech recognition from IHC output using MoS_2 FG-FET. a**, (LHS) The down sampled inner hair cell (IHC) output of dimension 54×108 for digits 0-9 in the TIDIGITS dataset is shown. (RHS) Spectogram of 54×108 synapses of each output neuron after training showing weight patterns which are similar to the original spectrograms (LHS). **b**, Confusion matrix and **c**, t-SNE visualization of the speech recognition task performed over TIDIGITS dataset.

the states of the MoS_2 memory, in an unsupervised manner.

$$w_{new} = w_{old} + \eta\ \Delta G\%,\ \ if\ \ 0.5 \times \tau_{+/-} \leq |\Delta t| \leq 4.5 \times \tau_{+/-} \quad (8)$$

The proposed neuromorphic hearing system is validated using isolated digits of the TIDIGITS database. The dataset consists of 6520 audio recordings of isolated digits 0 to 9, sampled at 20kHz, split equally into train and test set. Based on onset and offset of the spoken digit recording, all audios are fit into a 1 second time frame. The N-channel CAR model used to mimic cochlear behavior, takes the 1 second audio samples as input and based on the constant Q-filter parameters (Supplementary Section [I]), outputs the time-frequency mapping, i.e the spectrogram corresponding to the audio input. Here, we use 54-channel CAR model to extract frequency components within 100 Hz - 4 kHz range, as this range captures most of the speech information.

Fig. 5a (LHS) shows the CAR output spectrogram (54-channel × 20,000-samples) obtained for digits 0-9, respectively, down-sampled into 54 × 108 dimension to reduce the computational complexity on the neural network. Poisson neurons are used to model the response of the spiral ganglion neurons within the cochlea, to the down-sampled spectrogram. Each sample from the Poisson neuron's distribution is fed to the STDP neural network. The synapses in the STDP architecture learn connections from the Poisson neurons to the output integrate and fire (IF) neurons in an unsupervised manner. We use 16 IF neurons at the output, to capture various audio patterns within the down-sampled spectrogram of all digits. During the training phase of the neural network, the firing threshold of all IF neurons, $V_{threshold}$ is set as 1.5% of the energy in the input down-sampled spectrogram. This is done to compensate for the variation of energy within different digits, thereby ensuring uniform firing rate for all digits.

We adopt a winner-take-all strategy to update the synaptic connections, when IF neurons fire (details in Supplementary Section [II]). When more than one IF neuron fires simultaneously, the neuron with the highest membrane potential (the winner-neuron) is activated, and undergoes update based on STDP characteristics, to learn the input pattern. Since the input to the feature learning stage is the Poisson neuron response to the two-dimenisonal spectrogram, the learned synapses are also two-dimensional and of same size as that of down-sampled spectrogram (54×108). Once activated, the neuron enters its refractory period, within which the membrane potential of the neuron is reset to its initial state. This way, all the neurons compete with each other for activation. The IF neurons are further connected to each other with inhibitory connections. Thus, when an IF neuron fires, remaining IF neurons are forced to inhibit their membrane potential. Moreover, when none of the IF neurons fire, the membrane potential of all the neurons are decreased, so as to enhance competitive learning among the neurons.

The update value of synaptic connections ($\Delta G\%$ in Eq. 8) is influenced by the time difference between the Poisson neuron firing (pre-synaptic spike) and the IF neuron firing (post-synaptic spike). A time-continuous STDP function, as in Eq. 2 is defined, which best fits the MoS_2 memory device STDP characteristics (as shown in Fig. 3e). The STDP function is further quantized using the defined states of the memory device, and these are used to update the synapses for the digit recognition task under consideration. The STDP update is limited to $0.5 \times \tau_{+/-} \leq |\Delta t| \leq 4.5 \times \tau_{+/-}$, as was explained using Eq. 8.

Fig. 5a (RHS) shows the synapses obtained after training is done on the STDP architecture with the down-sampled spectrogram. The various patterns within the synapse shows that with STDP updates, each synapse learns different speech formants hidden in different frequency ranges of the spectrogram. For example, the high frequency information in digits 2, 3 and 8 around frequency channel 20 is captured dominantly by neurons 2, 7, 10 and 12 around the same channel. Whereas the energy of digits 4, 5 and 9 around frequency channel 30-40 is captured by neurons 2, 4, 6 and 14. The high frequency information of digit 1 is captured by neurons 8 and 13 only. Hence, we can conclude that the synapses learns patterns from spectrograms, few of which may be common among different spoken digits, and few of which differentiates them from one another. The accumulated post-synaptic potential (PSP) of all the 16 IF neurons, which indicates the correlation between the input spectrogram and the trained synapse of each IF neuron, can be used as an effective measure to classify the spoken digits.

The accumulated PSP of all the 16 IF neurons, for all 3260 spoken digits in the training set of TIDIGITS database, was used to train the linear SVM classifier in the final stage of the NSRS. The trained linear SVM provides 88.92% accuracy for the remaining 3260 spoken digits in the test set of the TIDIGITS database. Fig. 5b shows the confusion matrix for the speech recognition task performed. True label on the x-axis indicates the actual class/digit to which the audio belonged to, and the the predicted label on the y-axis indicates the class/digit the classifier predicted for the given audio. The higher value on the diagonal in the confusion matrix, therefore, indicates higher number of spoken digits were predicted correctly. Fig. 5c represents t-SNE visualization, a form of clustering representation of the the 3260 test audios. Each dot in the visualization represents an audio, defined by the 16 IF neuron's accumulated PSP, obtained after the feature learning stage for that audio. Audios of

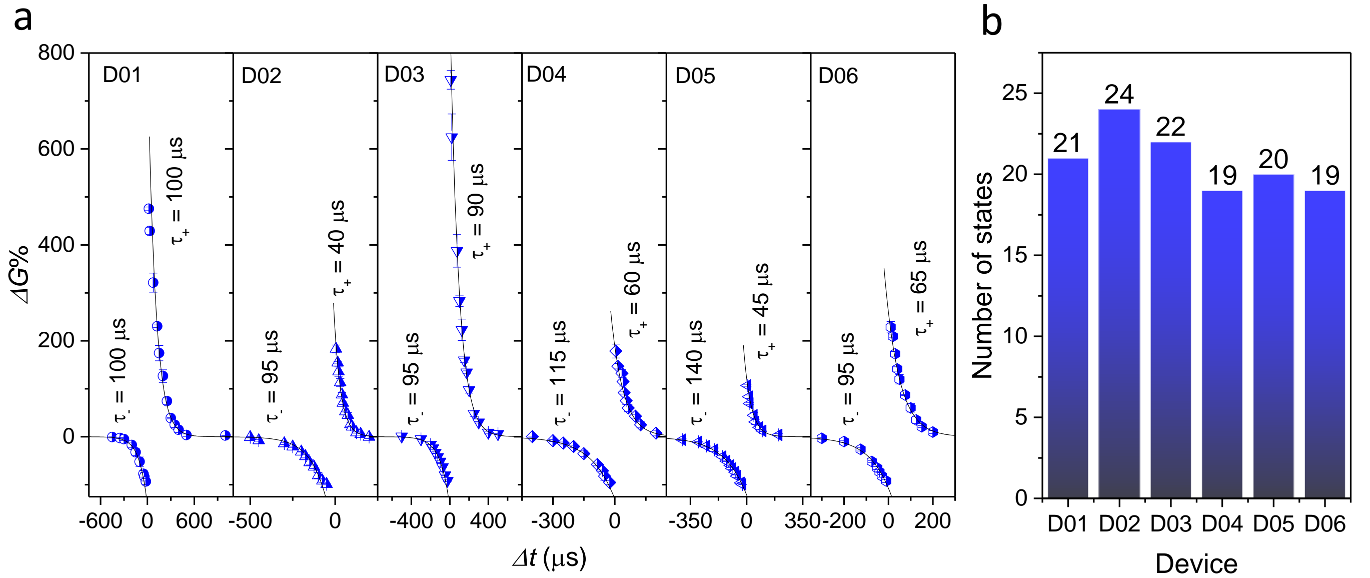

FIG. 6: **Device-to-device variation in STDP response**. **a**, Plots of STDP response for six MoS_2 FG-FETs. Black lines are exponential fits to the experimental data for measuring the decay timescale, while error bars indicate the spread of each state in the $\Delta G\%$ axis. **b**, Comparison of the number of states in different devices.

different spoken digits are represented using different colors. Hence, clusters of same color in the plot, represents how close the pattern of accumulated PSP of the output neurons are for audios belonging to same class/digit.

C. Device-to-device variation and its effect on neuromorphic speech recognition

We performed STDP measurements on six separate devices and the results depicting device-to-device variation are presented in Fig. 6. The STDP response shows a variation in both $\Delta G\%$ and time constant (τ_+ and τ_-) (Fig. 6a). Device-to-device variability can arise from numerous sources, however, in the case of MoS_2 FG-FET, this is mostly due to a variability in the mobility and contact resistance of the MoS_2 channel in different devices. A combination of these factors leads to a device-to-device variation in the maximum attainable conductance, and hence $\Delta G\%$ as well. The variability in time constant is a direct consequence of the variation in $\Delta G\%$, since devices with a larger overall change in conductance generally demonstrate higher time constants (Fig. 6a (Device D01 and D03) and Fig. 4d). Another possible source of mismatch is the variability in barrier injection height at the MoS_2/h-BN interface, which arises from defects and/or interfacial hydrocarbon formation (more commonly referred to as bubbles)[47] during the stacking process for fabricating the heterostructure. Removal of bubbles from heterostructure interfaces is still an ongoing effort in the two-dimensional device community, and effort was made in the current work to reduce the number of such disorders while fabricating the heterostructures. However, their effects, cannot be ruled out altogether. Alongwith the STDP response, the number of quantized states obtained per device also demonstrates slight variation (Fig. 6b). This number, which ranges between 19-24 for the devices measured, is obtained from the average spread of each state in the $\Delta G\%$ axis (Error bars in Fig. 6a). The spread/error in each state is determined statistically by computing the standard deviation from multiple (> 3) independent measurements at the same Δt. Our analysis shows a temporal sensitivity of $\approx 10 - 15$ μs in our synaptic devices. The variation in the number of quantized states is an important parameter and affects the quantization of the STDP function used for the cochlear recognition algorithm. A larger number of states is favourable and improves the capability of the NSRS in classifying different auditory inputs leading to better performance.

The performance of the NSRS was checked for device-to-device variation. Device mismatch was incorporated by a Gaussian distribution covering the range of timescales (τ_+ and τ_-) for the six measured devices, which were used to generate 54×108 STDP characteristics employed in updating the synapses. The speech recognition system is insensitive to device-to-device variation as indicated by the high rate of correct classification in the confusion matrix (Supplementary Section [VI]). We report an accuracy rate of 89.11% which is similar to the accuracy rate without including device mismatch. The robustness of our speech recognition system to device

mismatches is an important real-world-test as device-to-device variations are bound to exist in any fabrication process.

III. DISCUSSION

In this paper, we have demonstrated a MoS_2 memory device, with which a neuromorphic hearing system is developed and validated using the TIDIGITS audio database. The main novelty lies in demonstration and use of inherent plasticity of 2D-MoS_2 device to model the STDP rule as a synaptic memory, in a single device, without requiring any other learning circuitry. This is a significant advantage over other emerging memories, which only act as storage element. This reduces the computational complexity and memory requirement during training significantly as compare to conventional classification networks, which are based on back-propagation algorithm. The unsupervised feature learning stage learns low dimensional feature representation (in this case 16) from the input spectrogram, which makes our classifier very simple unlike traditional end-to-end supervised neural network architectures.

The proposed system has three major building blocks cochlea block, unsupervised feature extraction block and a linear classifier block. We have shown a novel neuromorphic architecture for machine hearing tasks applied to spoken digit recognition, but the system can be configured to learn for other auditory cognitive tasks such as speech recognition, speaker identifications and so on. We can envision the complete system integrated together using the three separate blocks in order to demonstrate the real time applications. We already have the in-house built cochlea model on FPGA[45], which can be interfaced with the 2D-MoS_2 based memory array to implement the STDP learning capability, followed by a linear classifier system[48–54]. The future work will be to integrate all these three separate systems on a single substrate.

IV. METHODS

To fabricate the MoS_2 FETs, we mechanically exfoliate MoS_2, h-BN and graphene on Si^{++}/SiO_2 (285 nm) substrate using the Scotch Tape method[55]. Exfoliated flakes are searched under an optical microscope. The thickness of hBN flakes are determined by atomic force microcscopy (AFM). The layer number of MoS_2 and crystallinity of graphene are verified using Raman spectroscopy[21]. **Selected flakes are aligned, stacked, and transferred onto a pre-patterned substrate using a home built micro-mechanical transfer setup. The polymer used for transfer is commercially available nail top coat solution (Lakme Color Crush), which shows good adhesion to two-simensional materials at temperatures between 60 and 120°C and is easily dissolved in acetone[56,57]. Electrical contacts to the MoS_2 channel and the extension of the FG are defined using electron beam lithography (EBL). For EBL, a double layer of commercially available electron beam resist, PMMA (Poly methyl methacrylate) (495PMMA A/950PMMA A MicroChem) with a total thickness of ~ 250 nm was spincoated on the device followed by exposure to electron beam. Subsequently, the patterns are developed in 1:3 MIBK:IPA, metallization is performed via thermal deposition of Cr (5 nm)/ Au (50 nm) in high vacuum (~ 10^{-6} mbar) conditions and excess metal is removed via lift-off in acetone. Electrical measurements are performed in vacuum at room temperature in a probestation (Lakeshore CPX-VF). For the transfer and output characteristics, two source meter units (SMUs) of the semiconductor parameter analyser (Keithley 4200A-SCS) was used to apply the V_{bg} and V_{sd}, while the current was measured using the SMU supplying the V_{sd}. For STDP measurements, the pre- and post-synaptic spikes are applied using two separate function generators (SRS DS 345) operated in the arbitrary function mode (ARB), fng_pre and fng_post, respectively. The pre- and post-spikes with defined Δt are loaded onto fng_pre and fng_post, respectively. To perform the measurement, the trigger out of fng_pre is connected to trigger in of fng_post. fng_pre is triggered using GPIB which triggers fng_post and two spikes with pre-determined time separation are applied. The resulting conductance change is obtained by measuring the current due to a small read voltage $V_{read} = 0.05$ V applied at the drain terminal using the Keithley 4200A-SCS.**

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VI. AUTHOR CONTRIBUTIONS

TP, KKT and AG planned the experiments on MoS_2 FG-FET devices. TP and KKT performed the experiments. AAM performed the cochlear recognition using NSRS. All authors contributed equally towards writing the manuscript. AG and CST conceived and supervised the project.

VII. COMPETING INTERESTS

The authors declare no competing interests

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