ASIC based LVDT Signal Conditioner for High-Accuracy Measurements*

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Abstract. A novel Application-Specific Integrated Circuit (ASIC) based signal conditioning system for closed loop control of Linear Variable Differential Transformer (LVDT) for sensor interface application is presented in this paper. The LVDTs are used for measuring linear displacement in industrial, military, aerospace, sub-sea, downhole drilling, nuclear power and process control applications. The signal conditioning is achieved through an ASIC-based digital signal processing unit. The existing commercially available Integrated Circuits (ICs) for LVDT signal conditioning are mostly analog and additional external circuitry is required for processing. The proposed system is a digital implementation of the LVDT signal conditioner with a better dynamic response and linearity through closed loop control. A unique feature of this ASIC is the use of synchronous demodulation technique using ADC sampling, reducing the complexity involved in conventional AM demodulation circuits. One of the major advantages of digital implementation is that the system can be reconfigured through external supervisory control. In this implementation, this is enabled by a universal asynchronous receiver-transmitter (UART) interface. This makes the system suitable for a wide range of applications. The functionality of the system was verified through a Verilog implementation on ARTIX-7 Field Programmable Gate Array (FPGA). The ASIC design is implemented in SCL-180 nm technology with an area 1mm X 1mm and the power utilization is 285 μW.

Keywords: LVDT · Signal Conditioner · ASIC.

1 INTRODUCTION

The linear variable differential transformer (LVDT) is a displacement transducer that accurately measures position and is extensively used in various industries for displacement measurement. The working principle of LVDT is detailed in

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[1]. Many applications require reading uncertainty as low as a few micrometers and also may require the transducer to be located in harsh and crammed environments, for instance, the case of the Large Hadron Collider (LHC) collimators position survey system [2]. In such cases, locating the reading electronics far from the transducer might tamper the accuracy. Further, locating the modules too near may not be possible due to space constraints. Such applications demand the signal conditioning module to be integrated with the transducer. As a result, a highly miniaturized and application specific module is necessary. Hence an ASIC based implementation is chosen. ASIC has several advantages over microcontroller/Digital Signal Processing (DSP) based solutions. ASIC is more suitable for hard real time applications as it is a hardware implementation and hence more deterministic whereas microcontroller/DSP requires software development. Also with the continuous increase in demand across industries, ASIC based solutions are economically more viable. The schematic of an LVDT integrated with an ASIC based signal conditioner is shown in Fig. 1. Other implementations of LVDT signal conditioner are discussed below.

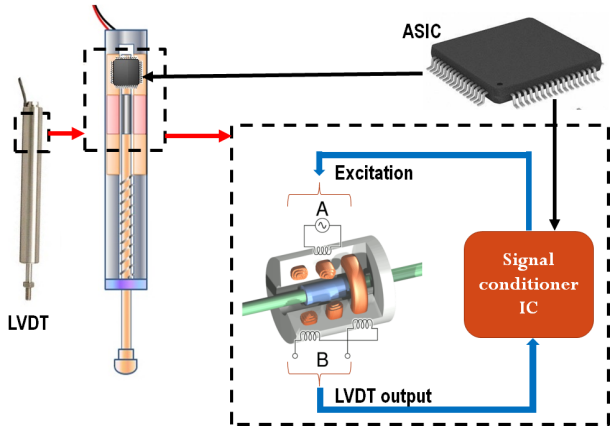

Fig. 1. LVDT integrated with signal conditioner ASIC

A Digital Signal Processing (DSP) based LVDT signal conditioner is presented in [1] and [9]. The FPGA based implementations of the LVDT are presented in [3], [11]-[14]. The paper [3] presents a phase compensated signal conditioner, while [11] presents a non-linearity compensator of an LVDT sensor based on Artificial Neural Network (ANN). The LVDT for various applications can be found in the literature. A high precision radiation LVDT conditioning presented in [10], [13]-[14] talks about the measurement of position, velocity and acceleration of a rotating shaft and [8] presents an accurate linear measurement using LVDT.

The LVDT output is a double sideband suppressed carrier amplitude modulated (DSBSC-AM) signal. The core displacement information is modulated by

the precision sine wave excitation signal, which is given to the transformer primary winding. The sine wave is generated using direct digital synthesis (DDS) [6]. The modulated signal is obtained at the differential output of the secondary winding.

The objective of LVDT signal conditioning system is to measure the output voltage from the modulated wave at the transformer secondary that represents the movement of the core. The measured output will undergo required signal processing and is transmitted serially. There are two existing, well-documented approaches for LVDT signal conditioning. One is the ratio-based method [3] and the other is the synchronous demodulation method [4]. The ratio-based method computes position as the ratio of the transformer secondary output and primary input excitation.

However, ratio-based methods are noisy and in case there is a sensor-induced phase lag in the secondary differential waveform, the secondary to primary ratio does not give an exact measure of position, and a phase correction is required to produce the correct output. The second approach applies the standard phase-sensitive demodulation technique to the LVDT secondary output, a DSBSC-AM waveform.

The scheme is insensitive to sensor induced phase errors. However, this scheme necessitates the use of high performance floating point DSPs, and hence, may not be commercially viable for single channel LVDT signal conditioning. Two commercially available monolithic LVDT signal conditioners are AD598 and AD698 from Analog Devices. The AD598 and AD698 utilize the ratio-based method and their implementation details are documented in their respective datasheets [4]-[5]. Both implementations generate a primary excitation that varies from 20 Hz to 20 kHz, and a dc voltage proportional to the LVDT core position. The AD598 is insensitive to sensor-induced phase errors. The AD698 requires external RC network to eliminate sensor-induced phase lag. The proposed system implements an LVDT signal conditioner based on phase synchronous demodulation. It is The sine wave for exciting the transformer primary winding, as well as the three-phase square wave for driving the motor connected to the core, are generated using Direct Digital Synthesis (DDS). The differential output at the secondary winding of the transformer is demodulated using digital synchronous demodulation technique. There is also closed loop control to make the system linear and more dynamic. UART interface is an additional feature for external communication. The system will send output and health monitoring data to an external monitoring module where the data analysis is carried out. Based on the analysis, appropriate control inputs can be sent to the system.

2 SYSTEM DESCRIPTION

The system block diagram is shown in Fig. 2. The DDS output, which is a sine wave at user-defined frequency ranging from 10 kHz to 20 kHz, is used to excite the LVDT primary winding. This waveform is functioning as the carrier wave for modulating the signal corresponding to the core movement. Based on

the core movement, the transformer secondary produces a modulated output. This output is given as input to the Analog to Digital Converter (ADC). The ADC is sampled at positive and negative peaks of carrier signal. The output is reconstructed using sample values at the positive peak and inverted sample values at the negative peak. Since the carrier signal is generated by the ASIC, the peak points are readily available. This synchronous method avoids complex operation

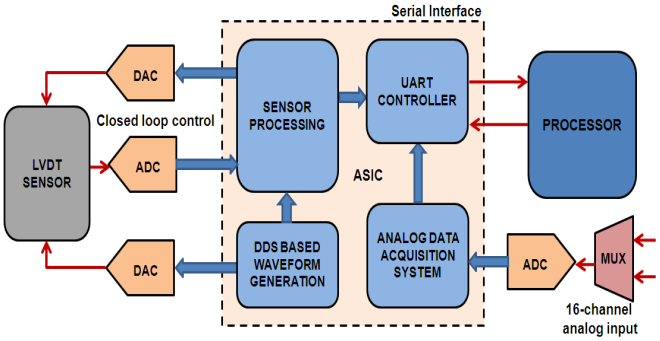

Fig. 2. Block diagram of the LVDT signal conditioning system

required for phase-sensitive demodulation architecture [7]. The demodulated output is applied to the filter and controller unit, which will remove unwanted harmonics signal present in the demodulated signal. The filtered output is fed to a controller for generating the necessary signal required for the closed loop control. This is to increase the dynamic range of the LVDT and also to increase the dynamic range of the system. The filtered output is decimated using a moving average filter and it is sent to an external monitoring system by a UART Transmitter. Health monitoring signals are also sent along with the filtered output. The UART Receiver module receives the control variables and filter coefficients from the external unit to get desired outputs.

3 COMPONENTS OF THE SYSTEM

The major components of the system are listed and explained in this section.

3.1 Direct Digital Synthesis (DDS)

Direct digital synthesis is a well-known technique for generation of standard waveforms. It basically is a look up table (LUT) based method where the sample values of the desired waveform are stored in an LUT and the user can generate the output waveform at the desired frequency required by the user. The block diagram describing DDS is shown in Fig. 3. The frequencies that can be obtained

are derived from the master clock (16 MHz) and the selection of the specific frequency is done by feeding a 4-bit input to this module. This method generates frequencies in the range 10 kHz to 20 kHz. The 4-bit input corresponds to the address of the LUT that stores the factor by which the master clock is to be divided to obtain the sampling rate corresponding to the desired frequency. The waveform of our interest is the sine wave input to the primary winding of the LVDT. In the second LUT 64 samples corresponding to this sine waveform is stored.

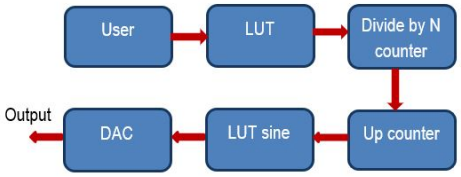

Fig. 3. DDS Module

3.2 Sensor Processing

The function of the sensor processing block, shown in Fig. 4, is to demodulate the sensor output, filter the output data for removing the unwanted harmonics and provide feedback signal for closed loop application. The data is decimated at a user-defined rate and is sent to the UART controller. The operation of ADC, DAC and multiplexer are controlled by timing control signals. The major functions of sensor processing module are explained below:

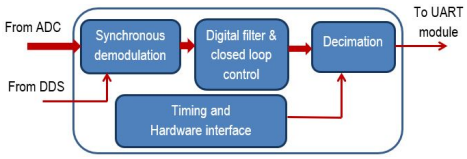

Fig. 4. Functional block diagram of the sensor signal processing

Phase-sensitive Demodulation

Phase-sensitive demodulation, also known as synchronous demodulation, is a technique for envelope detection of the modulated differential output signal received from the LVDT. The analog output from the LVDT is sampled periodically at the positive and negative peaks of the digitized modulated signal obtained from the ADC and the original carrier waveform from the DDS module are the inputs to this block. The carrier and the modulated waveform are multiplied for demodulation. The process involves sampling the negative peaks of the received signal and inverting it. Subsequently, the inverted negative samples are interleaved between the positive peak values to reconstruct the envelope. As discussed earlier, the envelope corresponds to the linear motion of the core of the LVDT. The pictorial representation of the above demodulation process and the obtained simulation response of the same in MATLAB and ModelSim are shown in Fig. 5, Fig. 6 and Fig. 7 respectively.

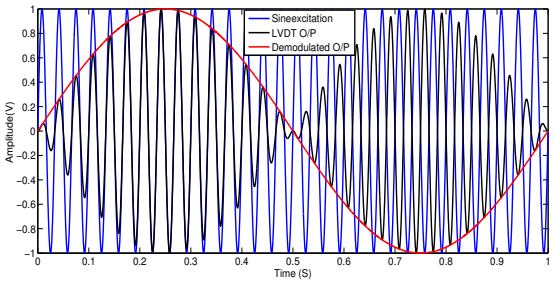

Fig. 5. Phase-sensitive demodulation technique

Digital Filter and closed loop control

An Infinite Impulse Response (IIR) filter is implemented in the system to filter the LVDT displacement signal. The transfer function of the IIR filter is shown in Fig. 8. In this module the command output generation for closed loop control of the LVDT core displacement is also implemented. The filter coefficients and control loop tuning parameters are fed into the system after calibration. The command signal is given to a torque generator to generate a force which prevents the core from moving outside its dynamic range. For obtaining the frequency response, the input signal frequency is varied with respect to time and filter output is plotted. The obtained simulation waveform is shown in Fig. 9.

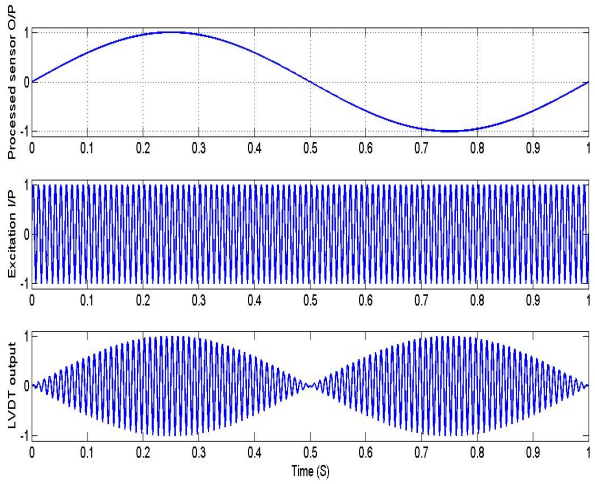

Fig. 6. Simulated response of the demodulation scheme in MATLAB

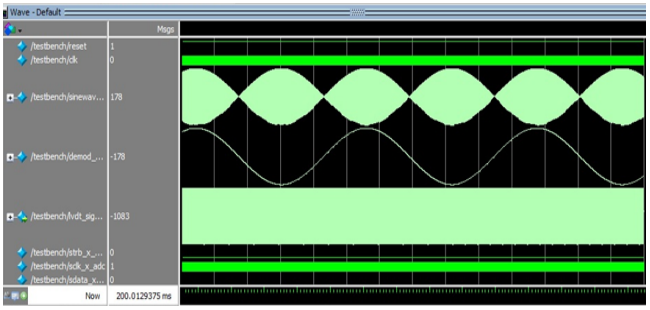

Fig. 7. Simulated response of the demodulation scheme in ModelSim

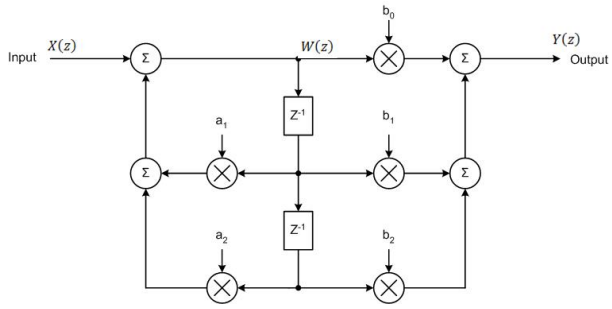

Fig. 8. IIR filter

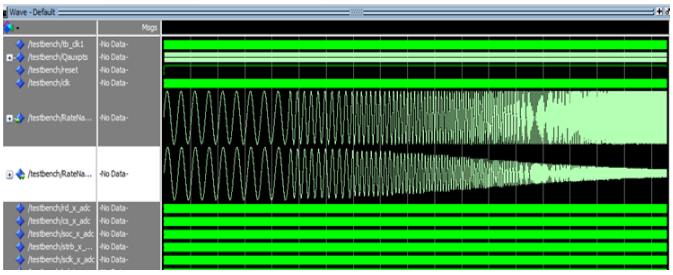

Fig. 9. Frequency response of IIR Filter

Decimation

The filtered output is available to this module at high data rate (10 KHz) with low resolution (10-bit). However the user requirement of the output will be normally low data rate (for example 50 Hz) with high resolution (typically 24-bit). The function of this module is to achieve these user requirements. This is done by using weighted block averaging. The precise timing signal for the decimation interval is generated by timing and hardware interface block shown in Fig. 4.

Timing and hardware interface

The function of timing block is to generate precise timing signals required for the hardware interfaces like ADC, DAC, multiplexer, etc. The same module will generate periodic pulses for the decimation interval. The ADC requires start of conversion, read and chip select pulses for the operation. Similarly, for closed loop operation, DAC write signal and data inputs are also to be provided. Also, control signals are to be generated for multiplexing the health monitoring channels for data acquisition. The simulated response of ADC interface is shown in Fig. 10. The interface is having clock, data and strobe signals. The data is sampled at the rising edge of the clock whenever the strobe signal is high.

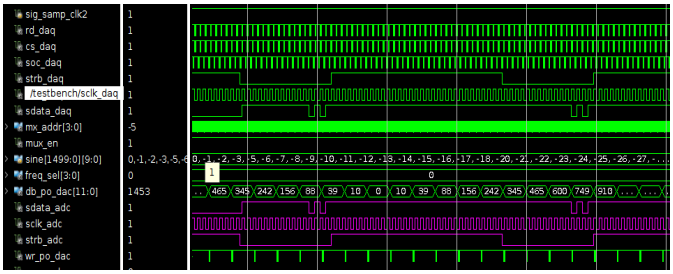

Fig. 10. Simulated response of ADC interface

3.3 System health monitoring

A number of critical health parameters are monitored and acquired along with the displacement information. These include power supply level status, temperature, reference voltage levels (data acquisition), carrier amplitude level, etc. The health parameters are analog signals, and a 16-channel analog multiplexer and ADC can be used along with the proposed ASIC for data acquisition.

3.4 Communication interface

The ASIC is implemented with a UART communication interface. The entire set of data, which includes the demodulated received signal, filter and control loop constants, health parameters, etc are packaged into packets and transmitted via the UART transmitter. The baud rate for the data transmission and reception is made selectable externally by the operator. As mentioned earlier, an operator can monitor the system parameters and provide supervisory correction inputs. The supervisory inputs could be received through the UART receiver module and will be used for the subsequent sensor output processing operation. The response of the UART transmission at a baud rate of 19.2Kbps at a periodicity of 20ms is shown in Fig.11.

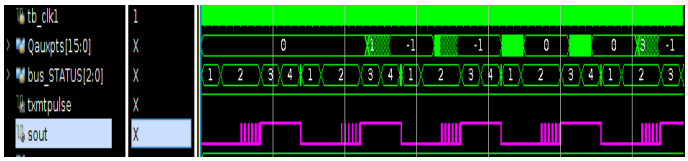

Fig. 11. Simulated response of UART module

4 IMPLEMENTATION

The standard ASIC design flow was followed for the design and implementation. The design flow is represented in Fig. 12. The register transfer level (RTL) implementation was done using verilog in Xilinx VIVADO environment. The various modules in the system were implemented and simulated using Modelsim. The logic was synthesized for ARTIX-7 FPGA and outputs were verified in the hardware. The RTL synthesis was carried out in Cadence environment using RTL compiler. The synthesis was performed for 100 MHz and timing margins were verified. The physical design was carried out in Cadence Encounter. The floor plan area was set based on the utilization of logic. Power and timing parameters were extracted from Cadence Encounter. The graphic data system (GDS) was streamed into Virtuoso after sign off checks. The design rule checks (DRC), layout versus schematic (LVS) and antennae violations were cleared using Calibre

SCL-rule deck. The final graphic data system (GDS) was streamed out from Virtuoso for tapeout.

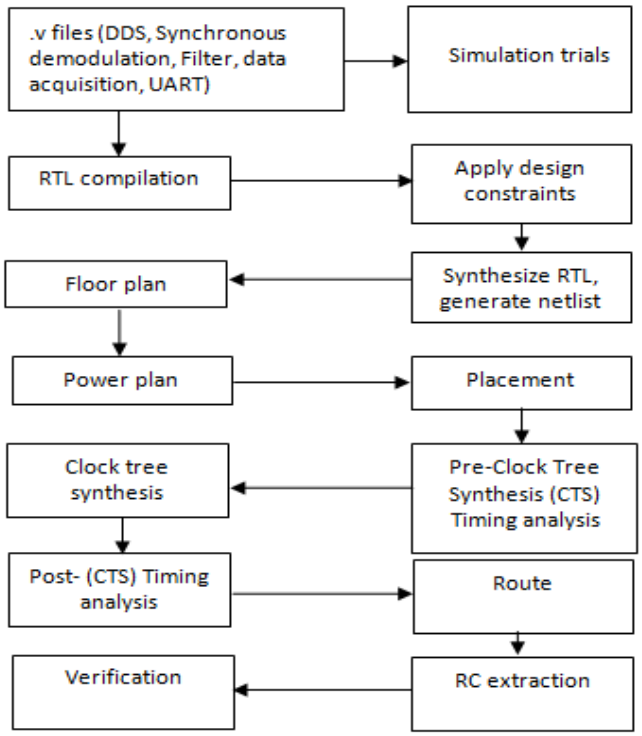

Fig. 12. ASIC design flow

5 RESULTS

The results obtained during physical design on cadence at the different stages like synthesis, timing analysis, power planning and verification are presented. The power plan report is given in Table 1. The timing analysis results were verified at all stages of physical design till sign off. The sign-off timing results for hold and setup analysis are separately shown in Table 2 and 3. The worst case negative slack (WNS) and total negative slack (TNS) are reported as positive in all the cases. The resource utilization of chip with CMOS SCL-180 nm technology and that on Artix-7 FPGA are shown in Table 4 and 5 respectively. The layout view of the GDS generated after verification is shown in Fig. 13

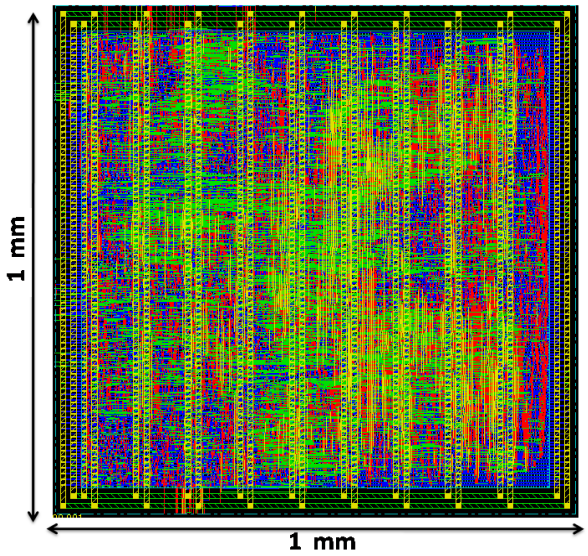

Fig. 13. Layout view of chip

Table 1. Power summary

Sl. No.	Title	Power (nW)
1	Cells	2976
2	Leakage	198.08
3	Internal	124340.01
4	Net	17220.26
5	Switching	141560.27

Table 2. Sign-off timing analysis report (hold)

Setup Mode	All	Reg2Reg	Default
WNS (ns)	3.634	4.439	3.634
TNS (ns)	≈ 0	≈ 0	≈ 0
Voilating paths	≈ 0	≈ 0	≈ 0
All paths	245	245	11

Table 3. Sign-off timing analysis report (setup)

Setup Mode	All	Reg2Reg	Default
WNS (ns)	0.020	0.070	0.020
TNS (ns)	≈ 0	≈ 0	≈ 0
Voilating paths	≈ 0	≈ 0	≈ 0
All paths	504	245	271

Table 4. Resource utilization of chip with CMOS SCL-180 nm technology

Instance	Cells	Cell Area	Net Area	Total Area
$LVDT\_sigconditnr$	9017	255267	143633	398901
$filter\_0$	7177	194501	118399	312900
dmux16_1	221	17292	1139	18431
$anlg\_daq\_0$	216	7994	2835	10829
$waveform\_gen\_1$	233	4858	3442	8300
$UART\_Transmitter\_0$	156	3559	2012	5572

Table 5. Resource utilization on Artix-7 FPGA

Sl. No.	Name of the module	Slice LUT	Slice registers
1	Analog data acquisition module	65	61
2	IInd order bi-quad IIR filter	51	192
3	Synchronous demodulation	113	93
4	UART Transmitter module	55	29
5	Waveform generation module	26	17
6	LVDT signal conditioner	1092	785

6 CONCLUSION

A novel ASIC-based digital signal conditioner for linear variable differential transducer is designed and developed. The design has been implemented in FPGA ARTIX-7 and the functionality verification was done after interfacing with LVDT sensor. Subsequently, ASIC design was done following the standard ASIC design methodology, in the Cadence environment. The developed signal conditioner provides a low power and miniaturized solution and offers a direct serial interface to the processor. The direct interface minimizes any possible interference to the sensitive output of the sensor. This makes it suitable for high precision applications. The programmability of the filter coefficients, baud rate of the data transmission and frequency selection of sine wave through external UART interface makes it a superior choice for a wide range of applications. The closed loop control provision implemented in the system helps in achieving better dynamic response and linearity. A 16-channel analog data acquisition system also has been implemented in the system which can be used for monitoring various health parameters associated with the sensor and its environment. The chip consumes 285 μW power and area of 1 mm^2 in SCL -180nm technology.

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